

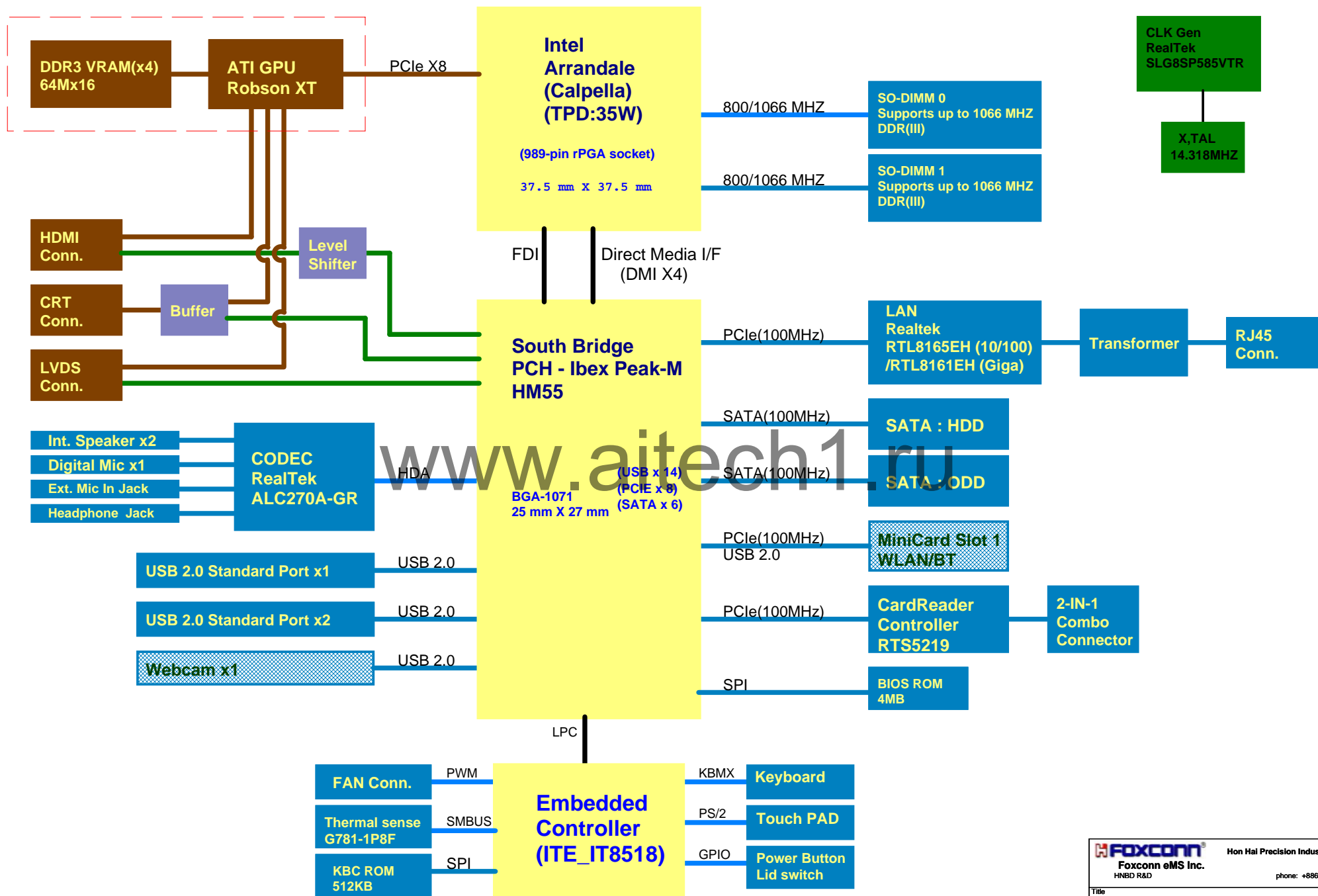
PROJECT NAME : CHICAGO (For Calpella MV Phase)

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05 -- POWER SEQUENCE	26 -- PCH (PCI,USB,NVRAM,GPIO)
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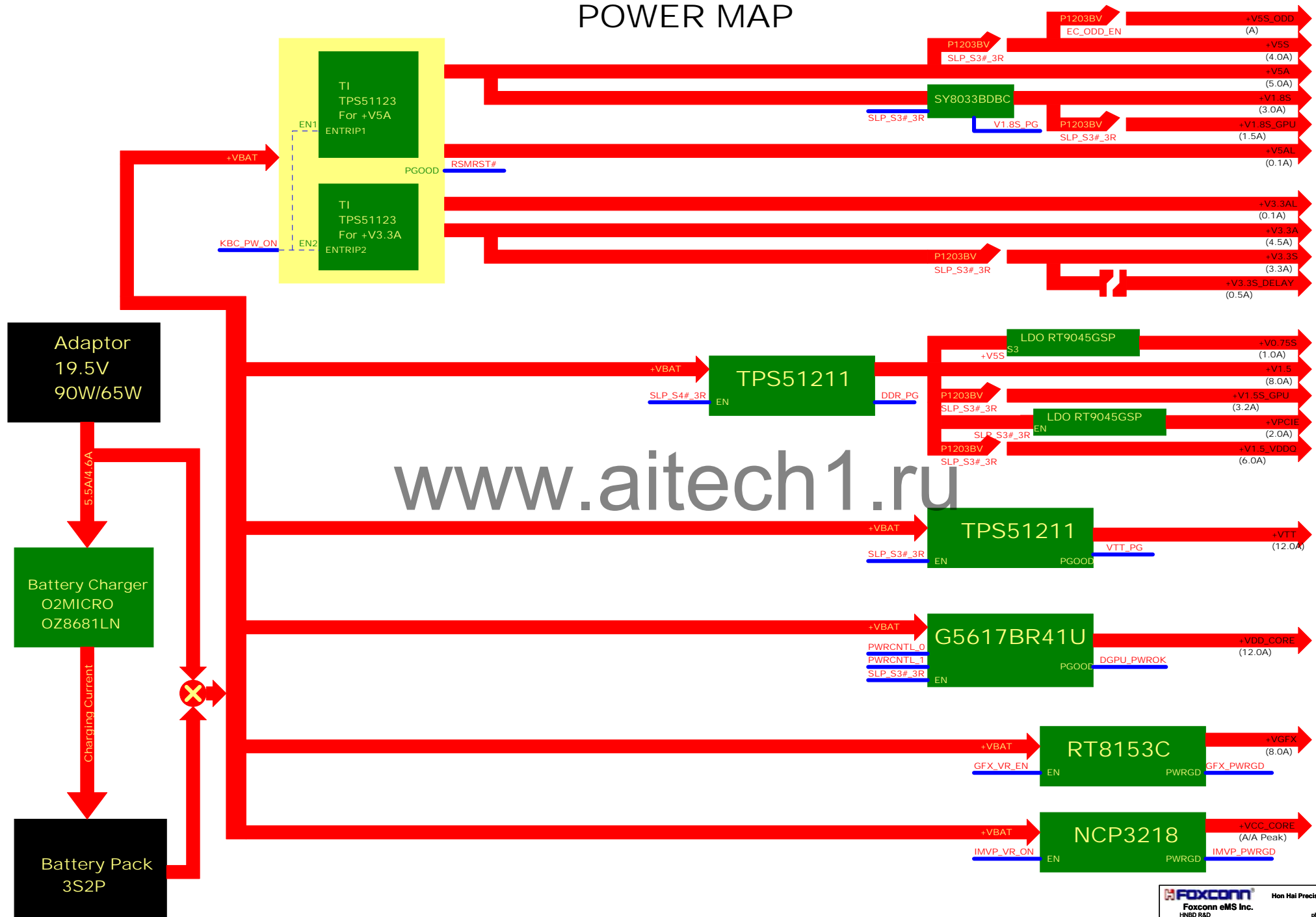
P. Leader	Check by	Design by

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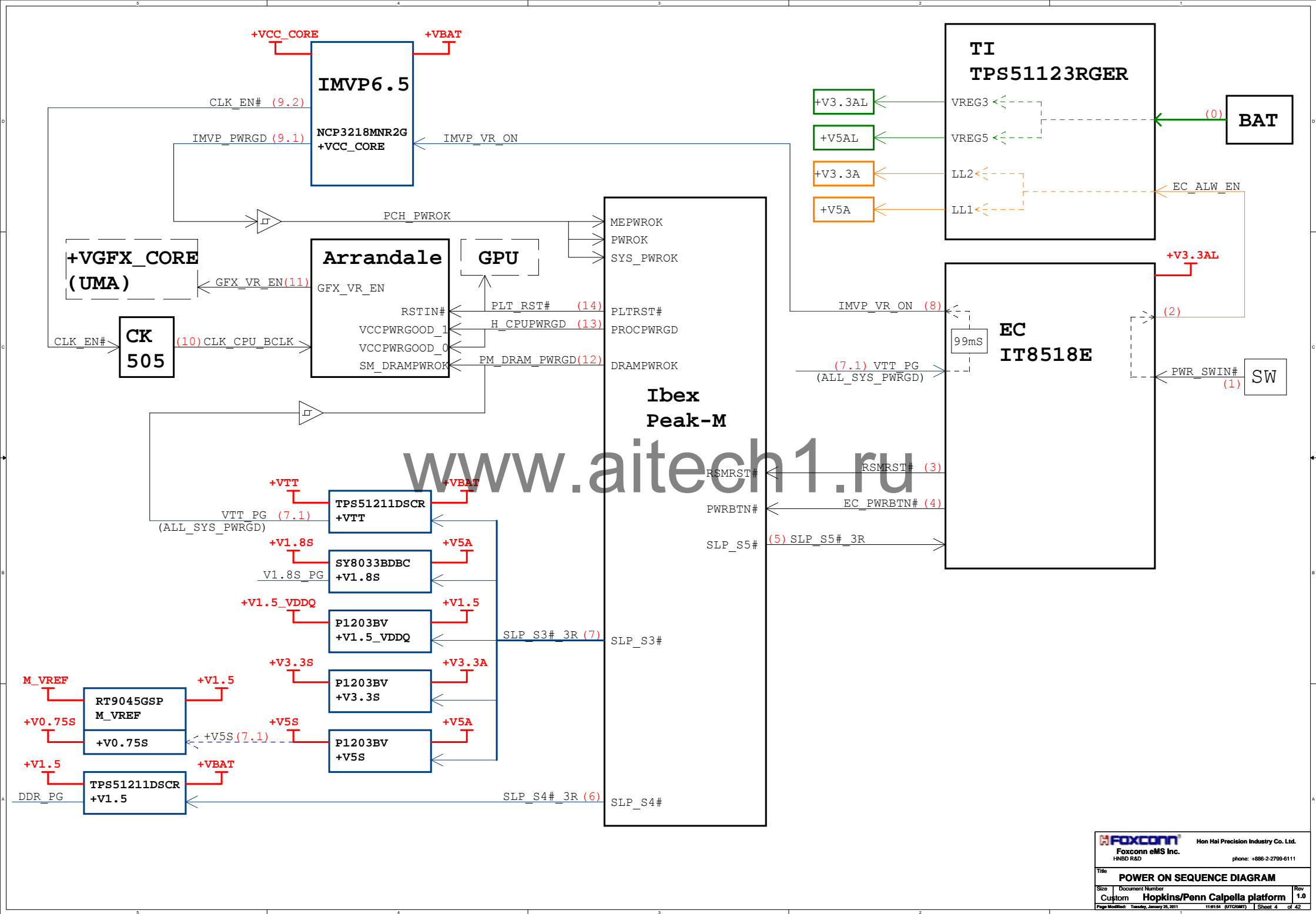
Title Index Page		
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POWER MAP

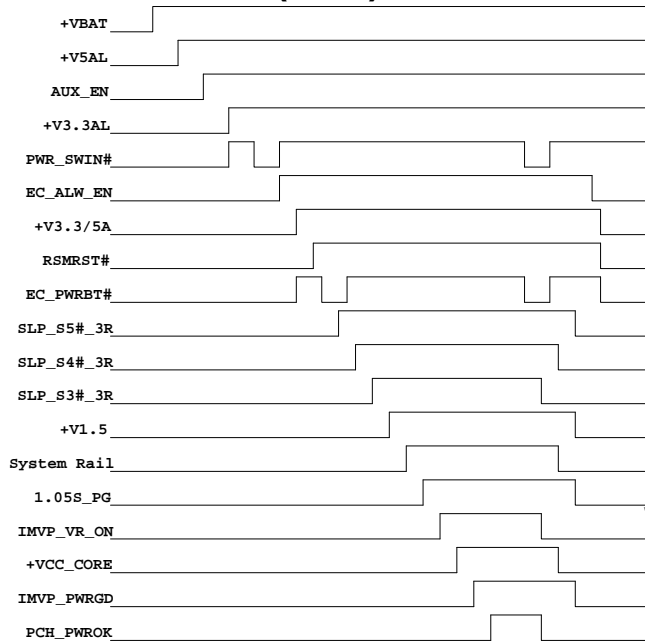


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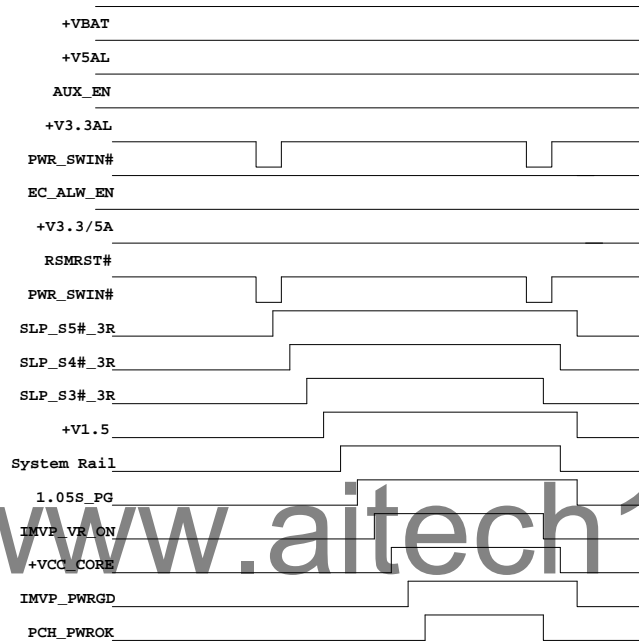


POWER SEQUENCE TIMING

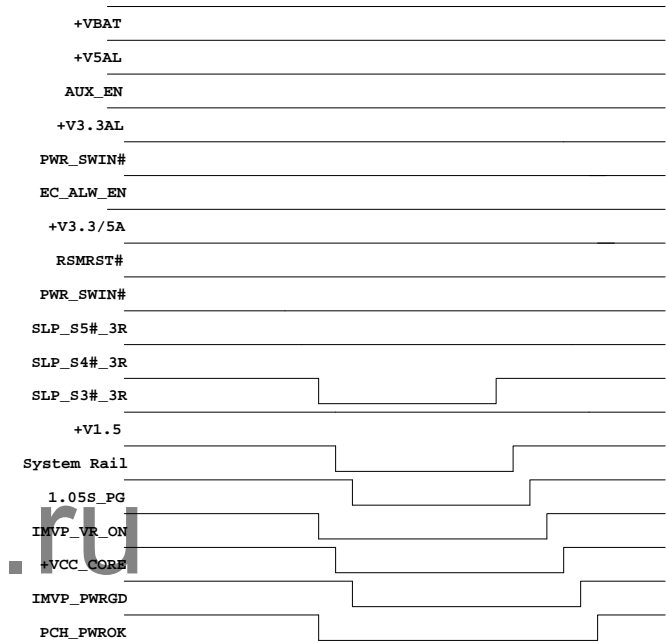
G3(OFF)->S0->S5



S5->S0->S5

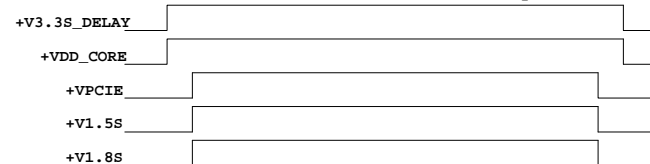


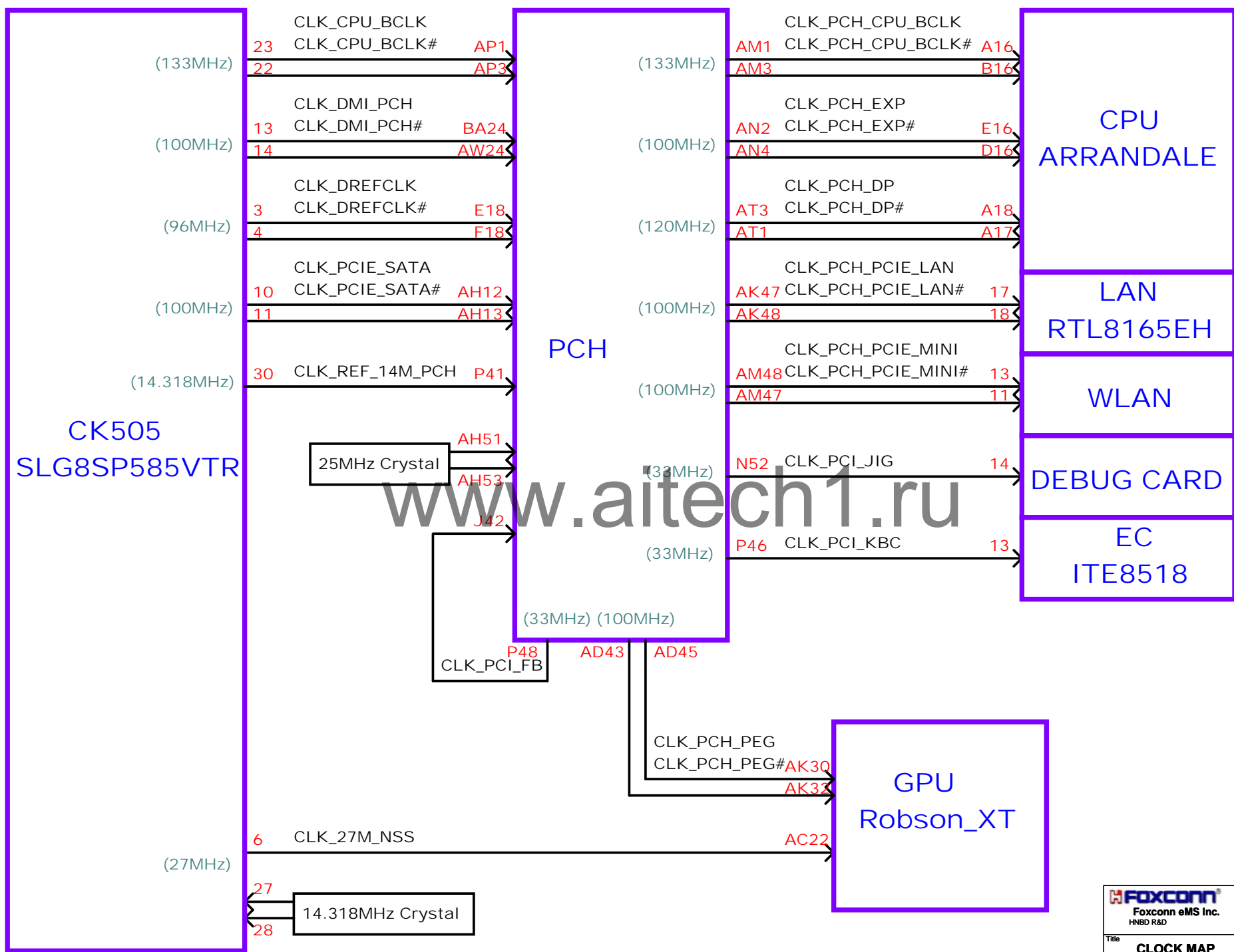
S0->S3->S0



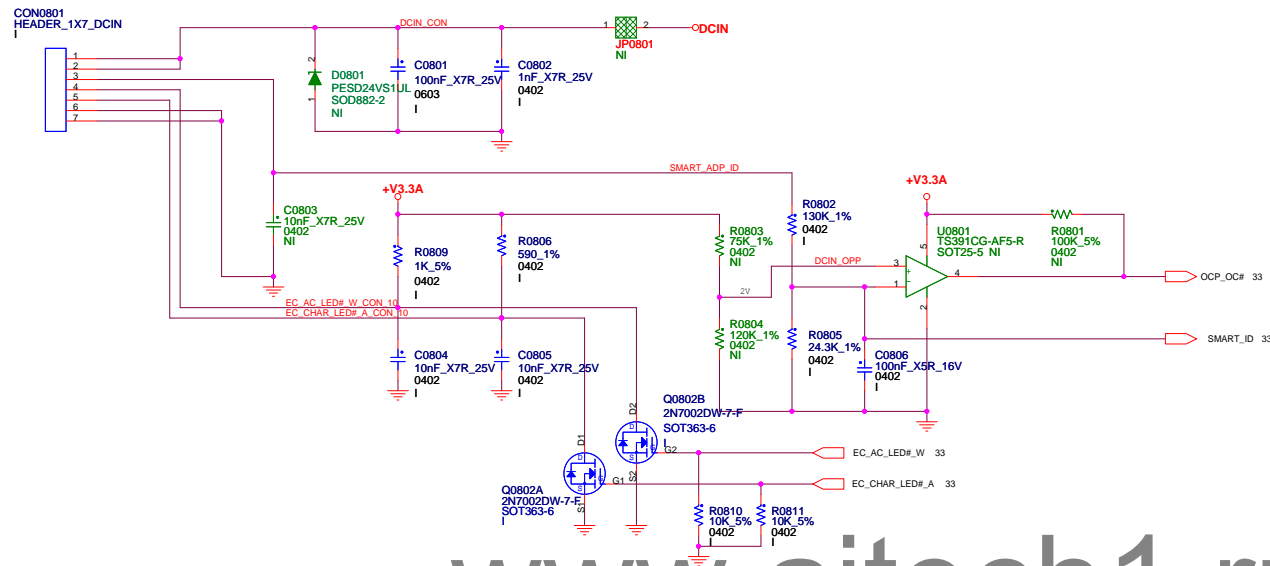
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GPU_Robson Sequence





DC_JACK WIRE to BOARD CONNECTOR

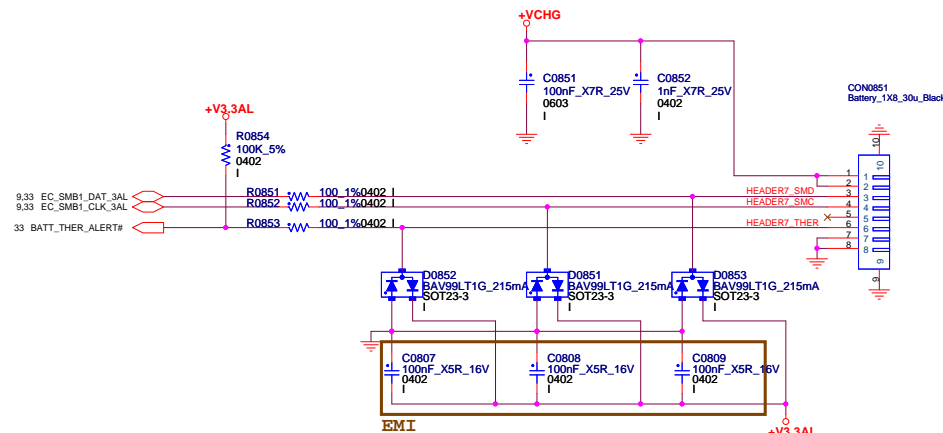


U0801 Pin1

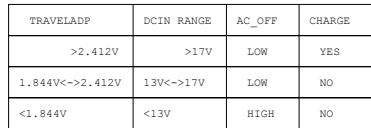
RID	65W/383K	90W/294K	120W/221K	135W/169K	180W/130K
SMART_ID	0.85~1V	1~1.1V	1.1~1.35V	1.35~1.55V	1.55~1.9V
ADPOCP	3V	3V	3V	3V	3V

DCIN_O	DCIN	9
+V3.3ALO	+V3.3AL	10,23,24,31,33,38
+V3.3AO	+V3.3A	10,14,15,18,23,24,25,26,27,33,35,36
+V3.3SO	+V3.3S	13,14,19,23,24,25,26,27,28,33,34,36,37,38,39,40,41,42

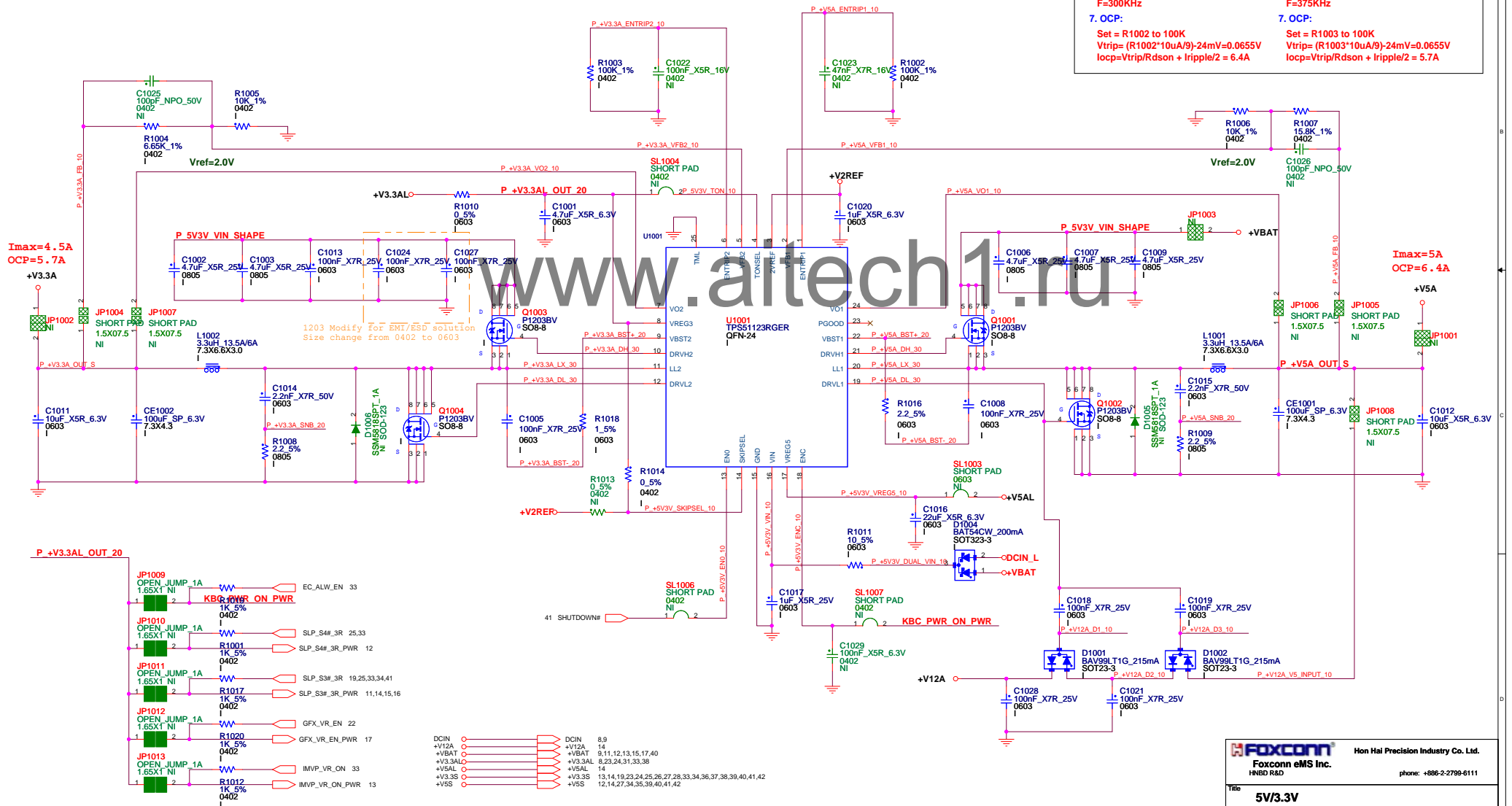
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BATTERY CONNECTOR



2011.0110.0



2011.0110.0



+VTT POWER SUPPLY

+VTT:

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.86A$$

2. Ripple Current:

$$I_{rip} = 3.42A$$

3. Ripple Voltage:

$$ESR/1 = 9m\Omega$$

$$V_{rip} = 30.78mV$$

4. Inductor Spec:

$$I_{sat} = 36A$$

$$I_{dc} = 18A$$

$$DCR = 3.3m\Omega$$

5. MOSFET Spec:

H-side MOSFET: IRF8707PBF L-side MOSFET: IRF8707PBF

$$R_{ds(ON)} = 14.2m\Omega \quad (V_{gs} = 4.5V) \quad R_{ds(ON)} = 14.2m\Omega \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 11A \quad (T = 25^\circ C) \quad I_{cont} = 11A \quad (T = 25^\circ C)$$

$$I_{peak} = 88A \quad (Pause = 10us) \quad I_{peak} = 88A \quad (Pause = 10us)$$

6. Frequency:

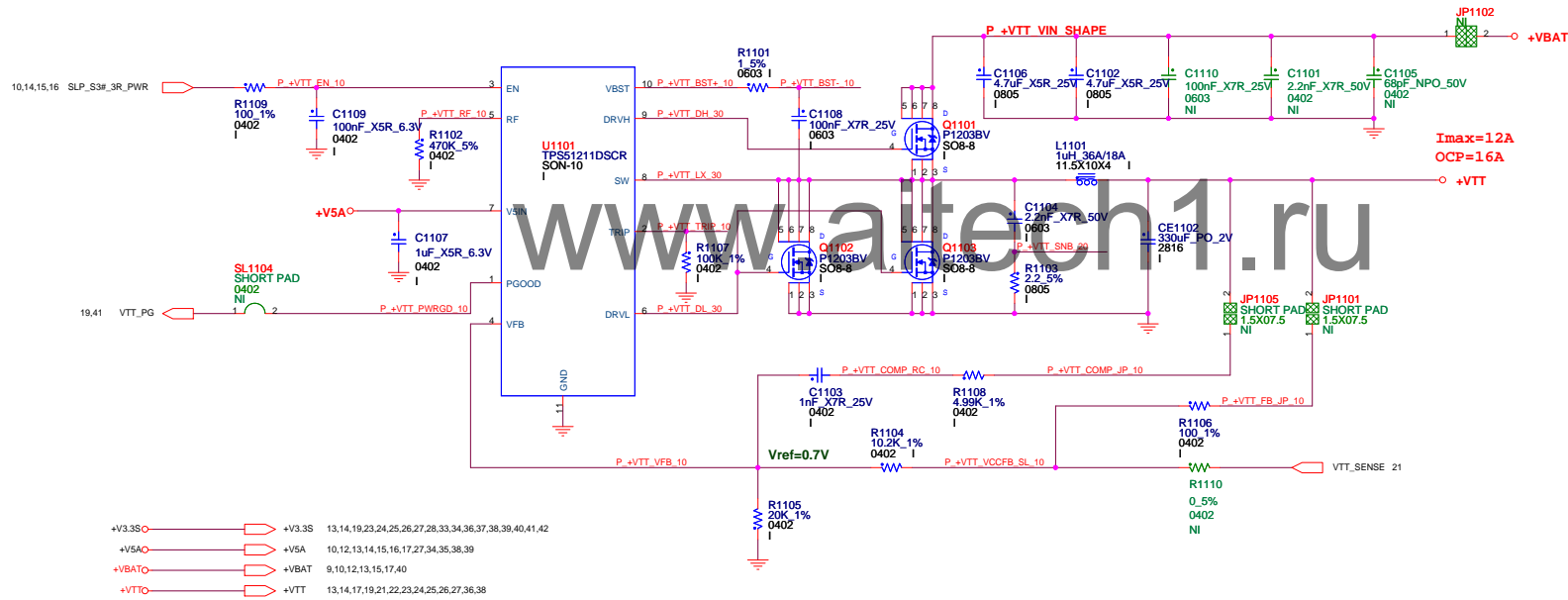
$$F = 290KHz \quad (R1102 = 470K)$$

7. OCP:

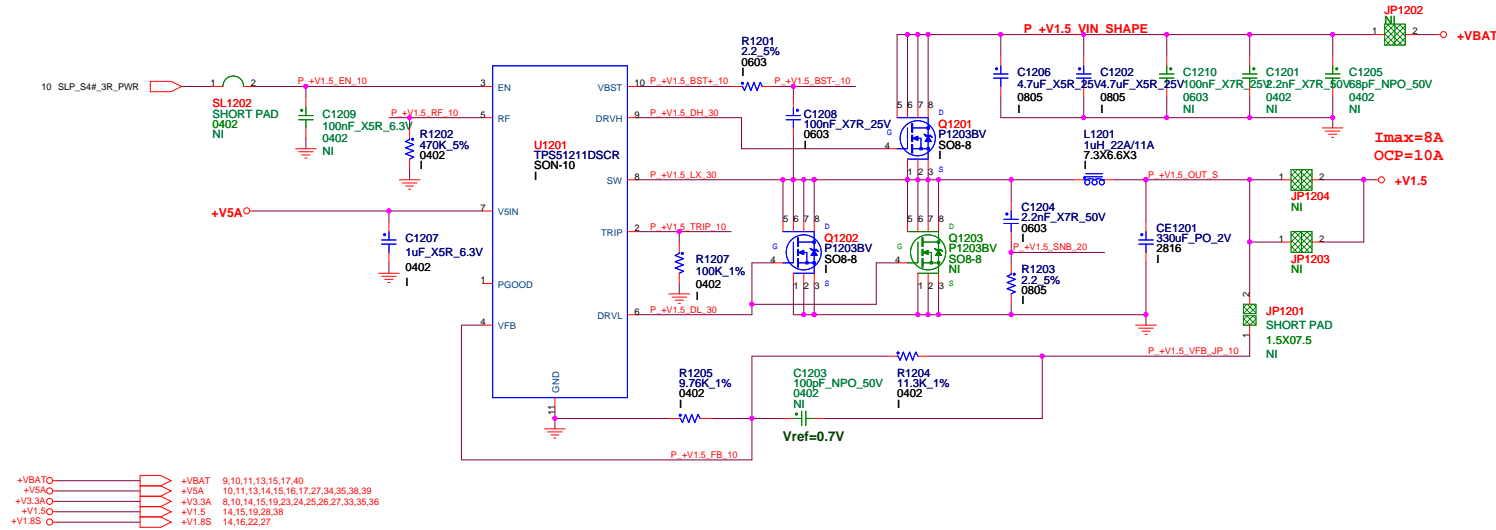
$$Set = R1107 \text{ to } 100K$$

$$V_{trip} = R1107 \cdot 10uA = 1V$$

$$I_{ocp} = (V_{trip} / 8 \cdot R_{ds(on)}) + I_{ripple} / 2 = 16A$$



+V1.5 POWER SUPPLY

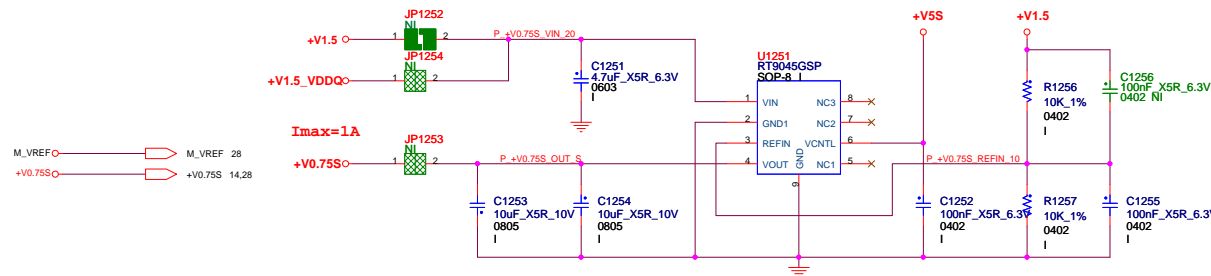


- +V1.5:**
- 1. I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.78A$
 - 2. Ripple Current:**
 $I_{rip} = 4.76A$
 - 3. Ripple Voltage:**
 $ESR/1 = 9m\Omega$
 $V_{rip} = 42.88mV$
 - 4. Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3m\Omega$
 - 5. MOSFET Spec:**
 H-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 14.2m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
 L-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 14.2m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
 - 6. Frequency:**
 $F = 290KHz$ ($R1202 = 470K$)
 - 7. OCP:**
 Set = R1207 to 100K
 $V_{trip} = R0907 \cdot 10uA = 1V$
 $I_{ocp} = (V_{trip} / 8 \cdot R_{dson}) + I_{ripple} / 2 = 10A$

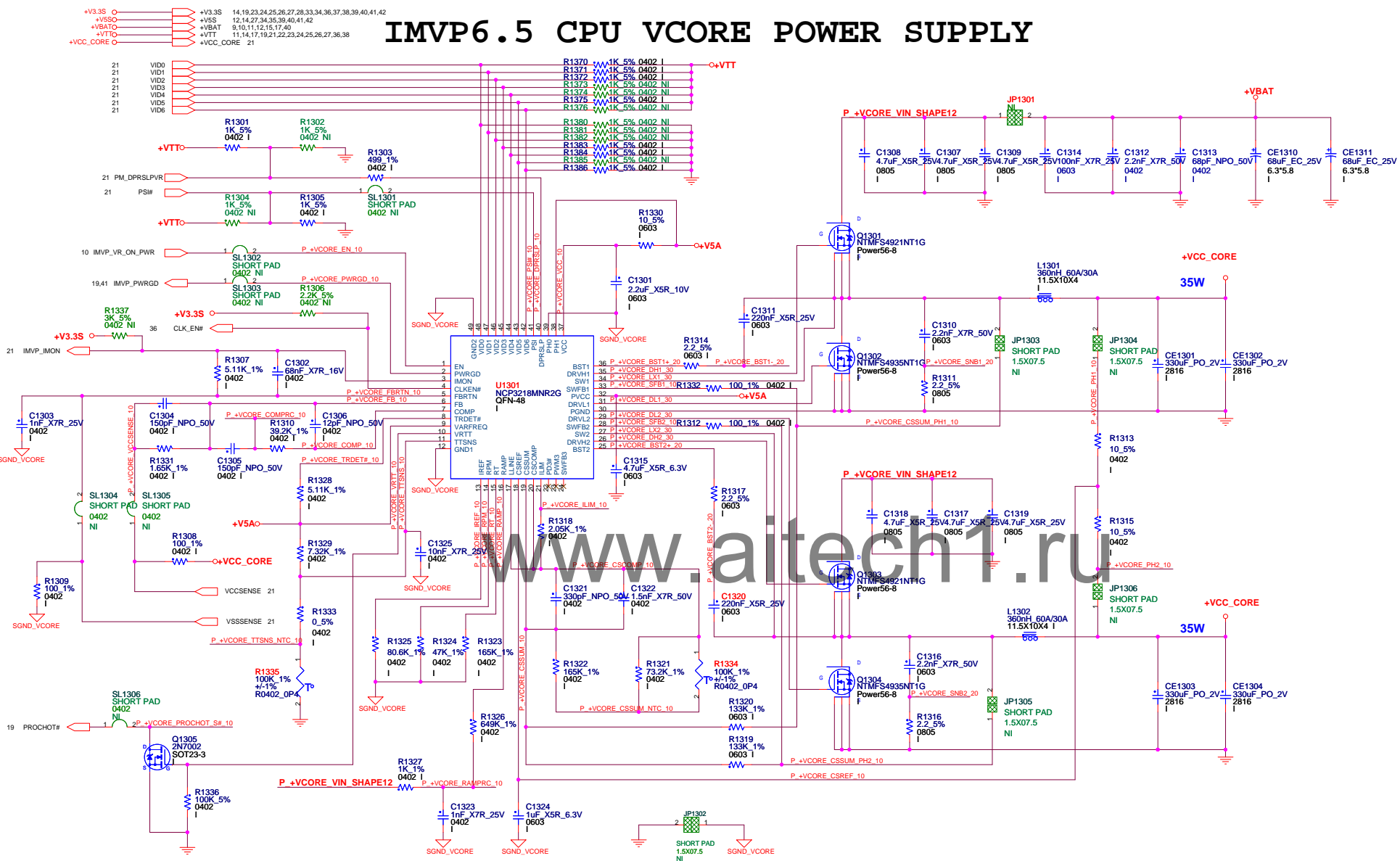
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+V0.75S POWER SUPPLY

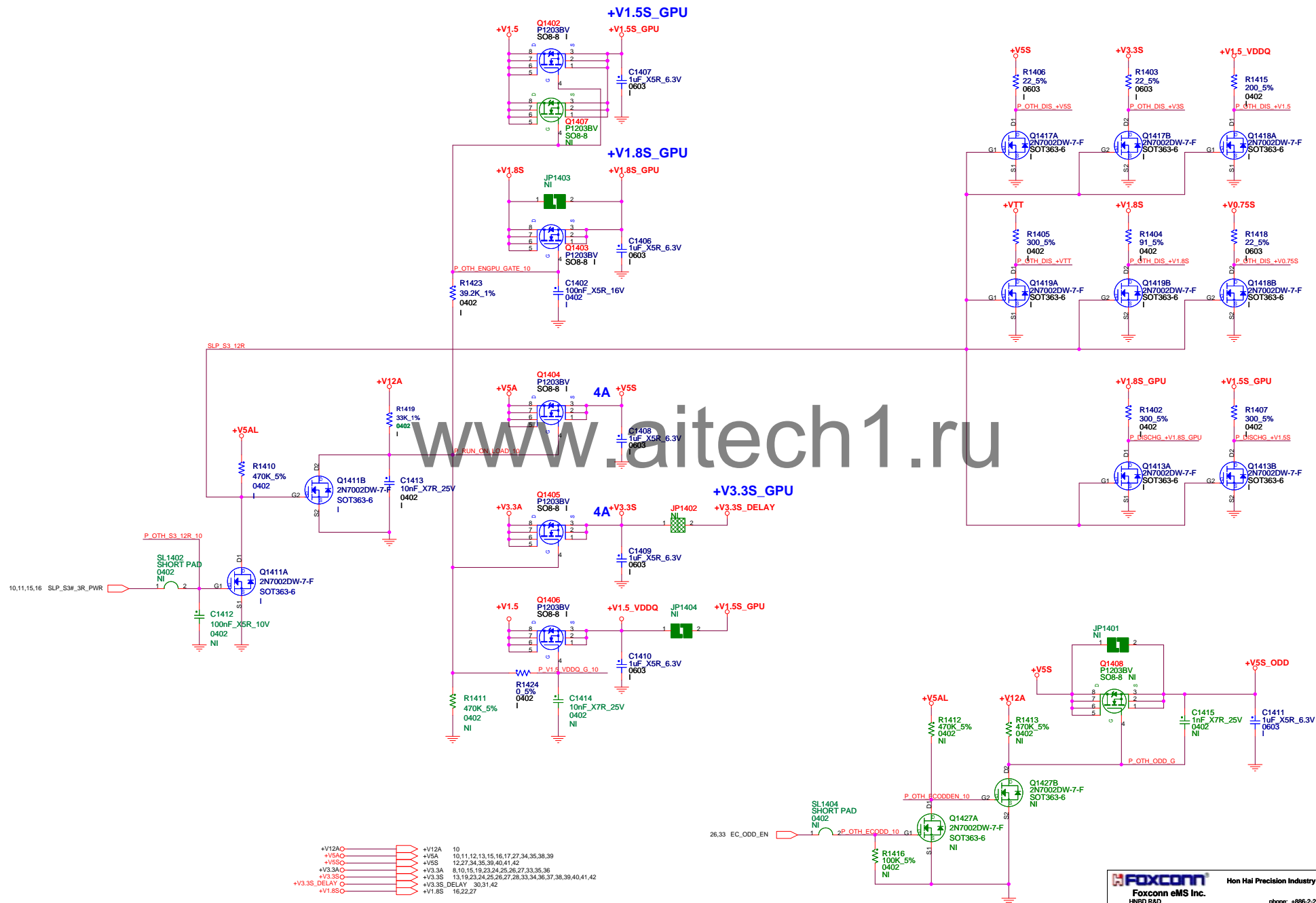
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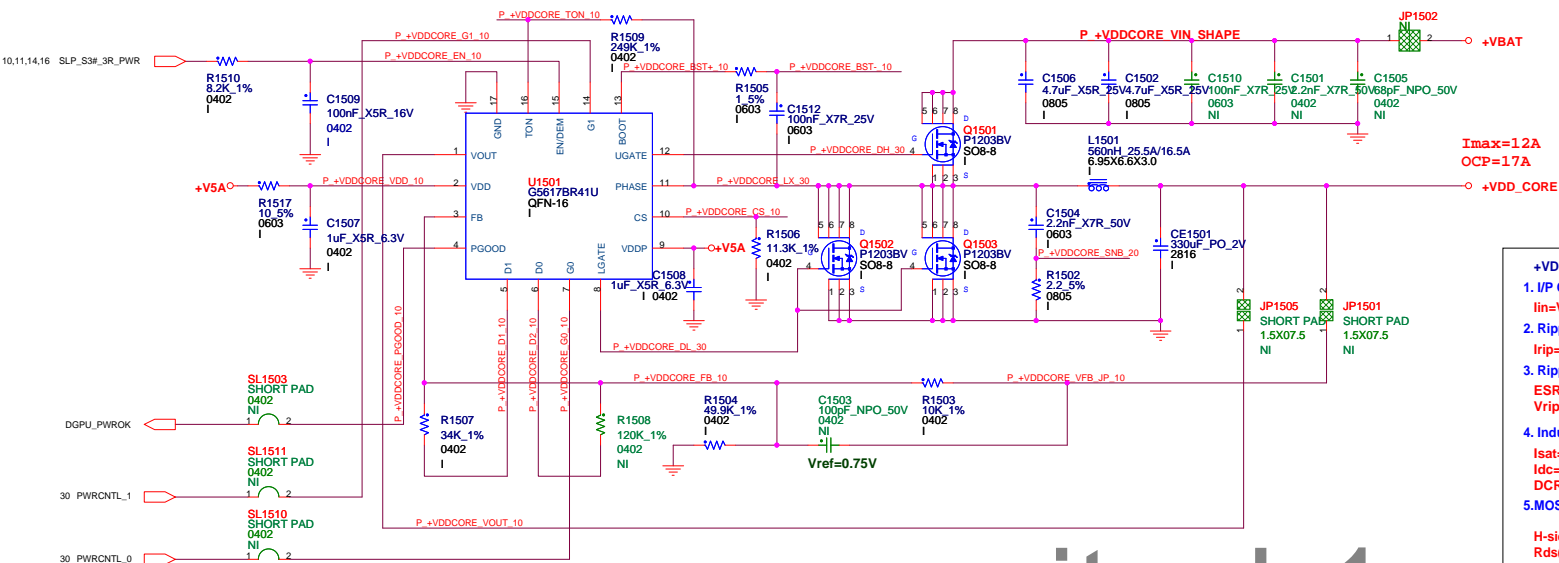
IMVP6.5 CPU VCORE POWER SUPPLY



OTHER POWER / DISCHARGE CIRCUITS



+VDD_CORE POWER SUPPLY



PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

+VDD_CORE:

1. I/P Current:

$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.48A$

2. Ripple Current:

$I_{rip} = 6.58A$

3. Ripple Voltage:

$ESR = 1 = 9m\Omega$

$V_{rip} = 59.22mV$

4. Inductor Spec:

$I_{sat} = 36A$

$I_{dc} = 18A$

$DCR = 3.3m\Omega$

5. MOSFET Spec:

H-side MOSFET: IRF8707PBF

$R_{ds(ON)} = 14.2m\Omega$ ($V_{gs} = 4.5V$)

$I_{cont} = 11A$ ($T = 25^\circ C$)

$I_{peak} = 88A$ ($\text{Pause} = 10\mu s$)

L-side MOSFET: IRF8707PBF

$R_{ds(ON)} = 14.2m\Omega$ ($V_{gs} = 4.5V$)

$I_{cont} = 11A$ ($T = 25^\circ C$)

$I_{peak} = 88A$ ($\text{Pause} = 10\mu s$)

6. Frequency:

$F = 290KHz$ ($R12509 = 294K$)

7. OCP:

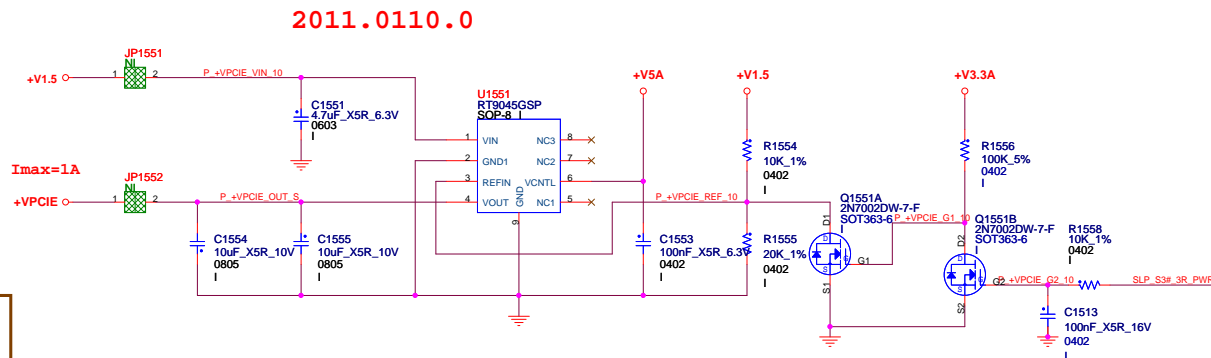
Set = $R1506$ to $11.3K$

$V_{trip} = R1506 \cdot I_o = 0.113V$

$I_{ocp} = (V_{trip} / R_{ds(on)}) + I_{ripple} / 2 = 16.2A$

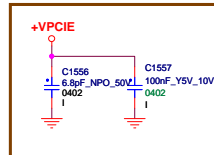
+VPCIE POWER SUPPLY

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+VBA_T	+VBA_T	9,10,11,12,13,17,40
+VSA	+VSA	10,11,12,13,14,16,17,27,34,35,38,39
+VSS	+VSS	12,14,27,34,35,39,40,41,42
+V3.3S	+V3.3S	13,14,19,23,24,25,26,27,28,33,34,36,37,38,39,40,41,42
+V3.3A	+V3.3A	8,10,14,19,23,24,25,26,27,33,35,36
+V1.5	+V1.5	12,14,19,28,38
+VDD_CORE	+VDD_CORE	31
+VPCIE	+VPCIE	29,30,31

EMI



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Title: VATVDD+VPCIE

Size: Document Number

C Hopkins/Penn Calpella platform

Page Modified: Tuesday, January 25, 2011 11:12:11 (UTC+08:00) Sheet 15 of 42

+V1.8S POWER SUPPLY

+V1.8S:

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.44A$$

2. Ripple Current:

$$I_{rip} = 0.53A$$

3. Ripple Voltage:

$$ESR/3 = 3.3m\Omega$$

$$V_{rip} = 1.75mV$$

4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 20m\Omega$$

5. MOSFET Spec:

H-side P-MOSFET:

L-side N-MOSFET:

$$R_{ds(ON)} = 110m\Omega \quad (V_{gs} = 4.5V)$$

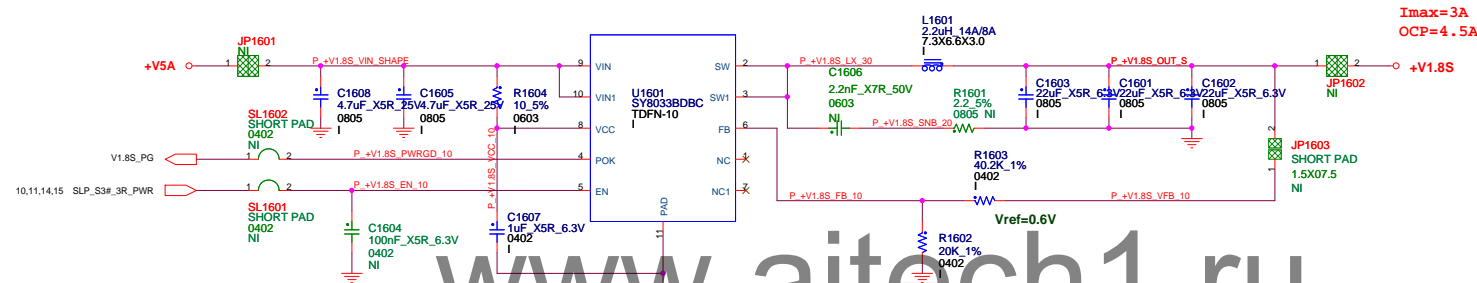
$$R_{ds(ON)} = 75m\Omega \quad (V_{gs} = 4.5V)$$

6. Frequency:

$$F = 1MHz \quad (\min = 800KHz, \max = 1.2MHz)$$

7. OCP:

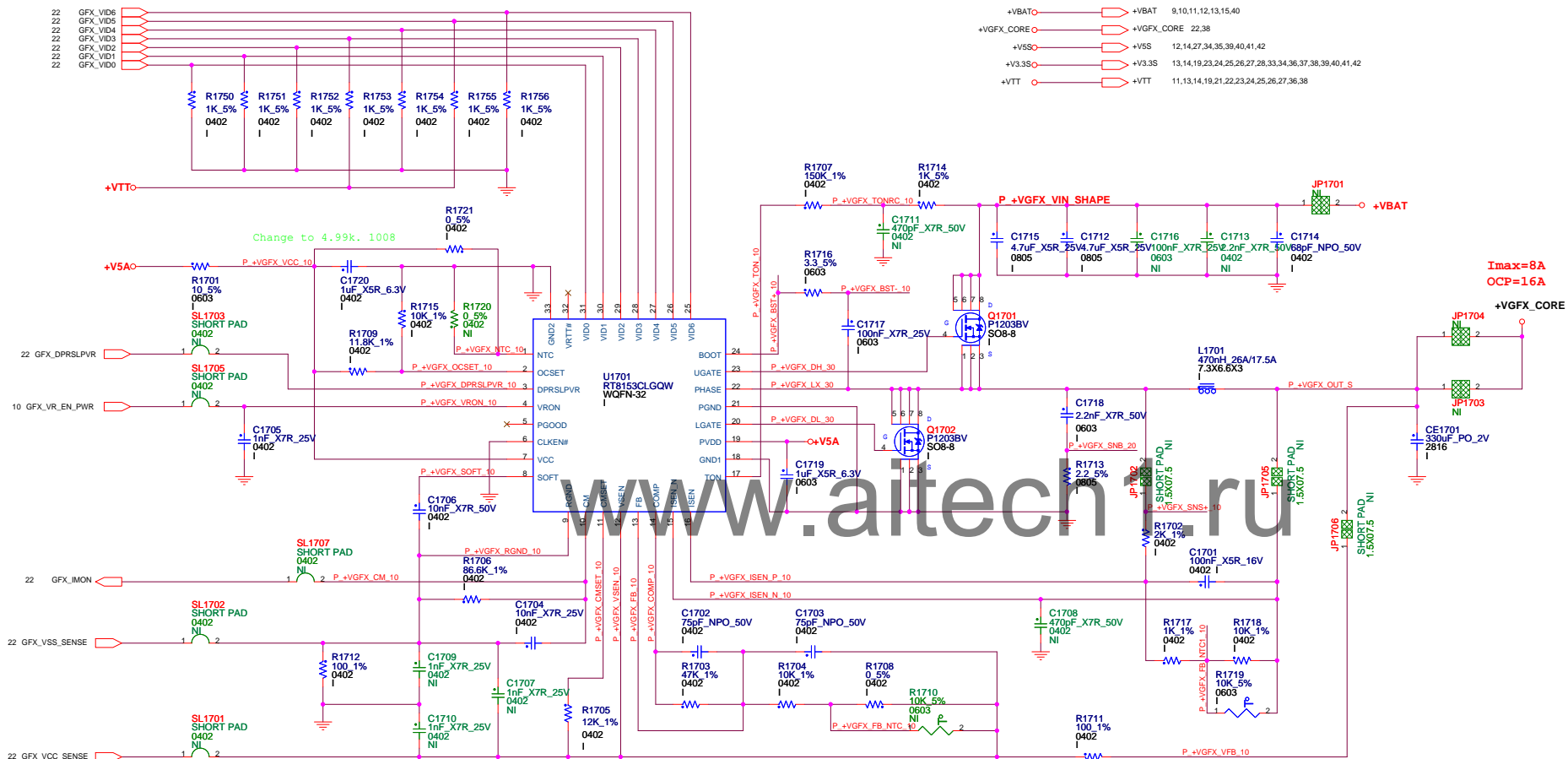
$$I_{ocp} = 4A(\min) / 4.5A(\text{typ}) / 5A(\max)$$

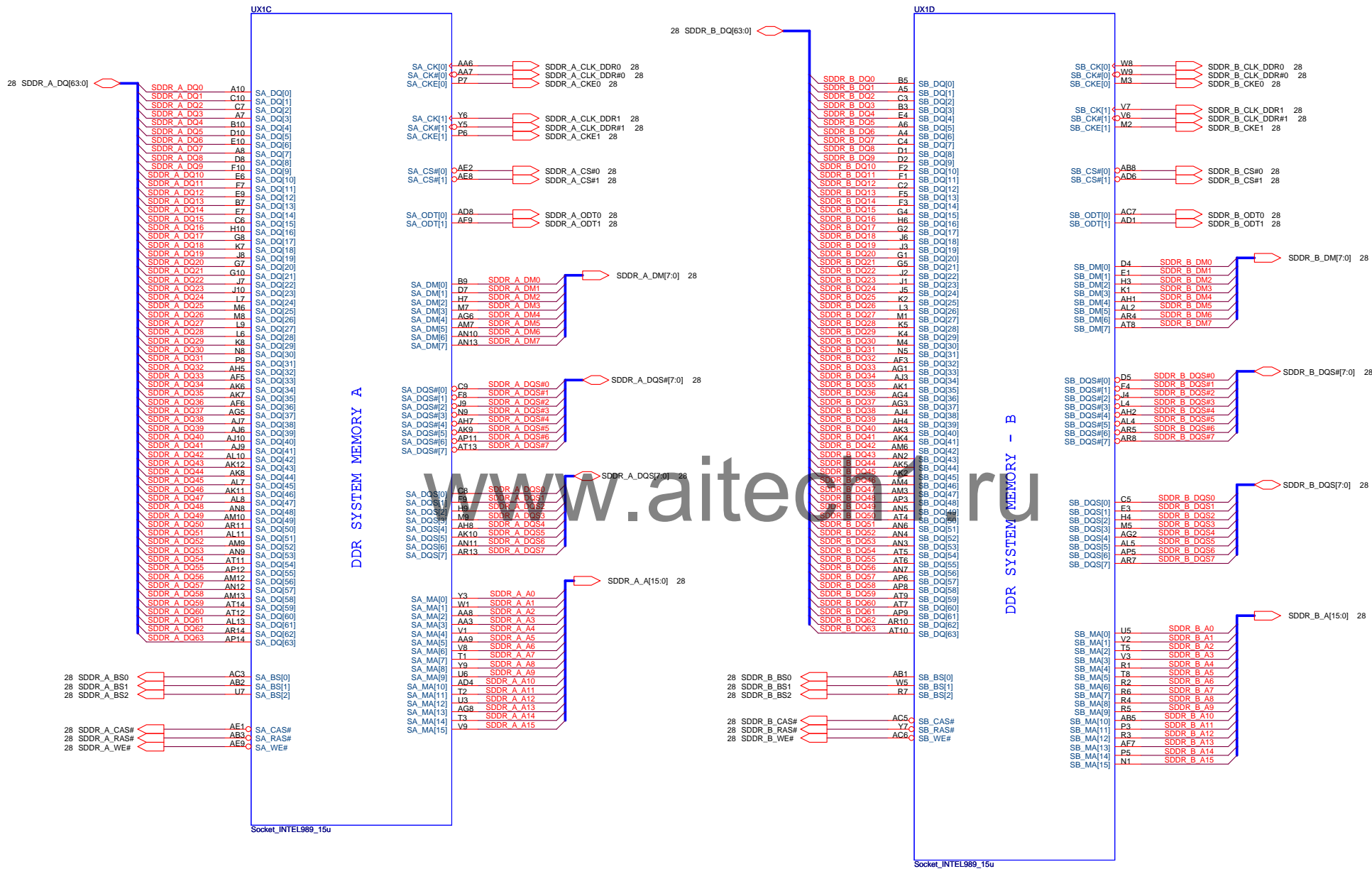


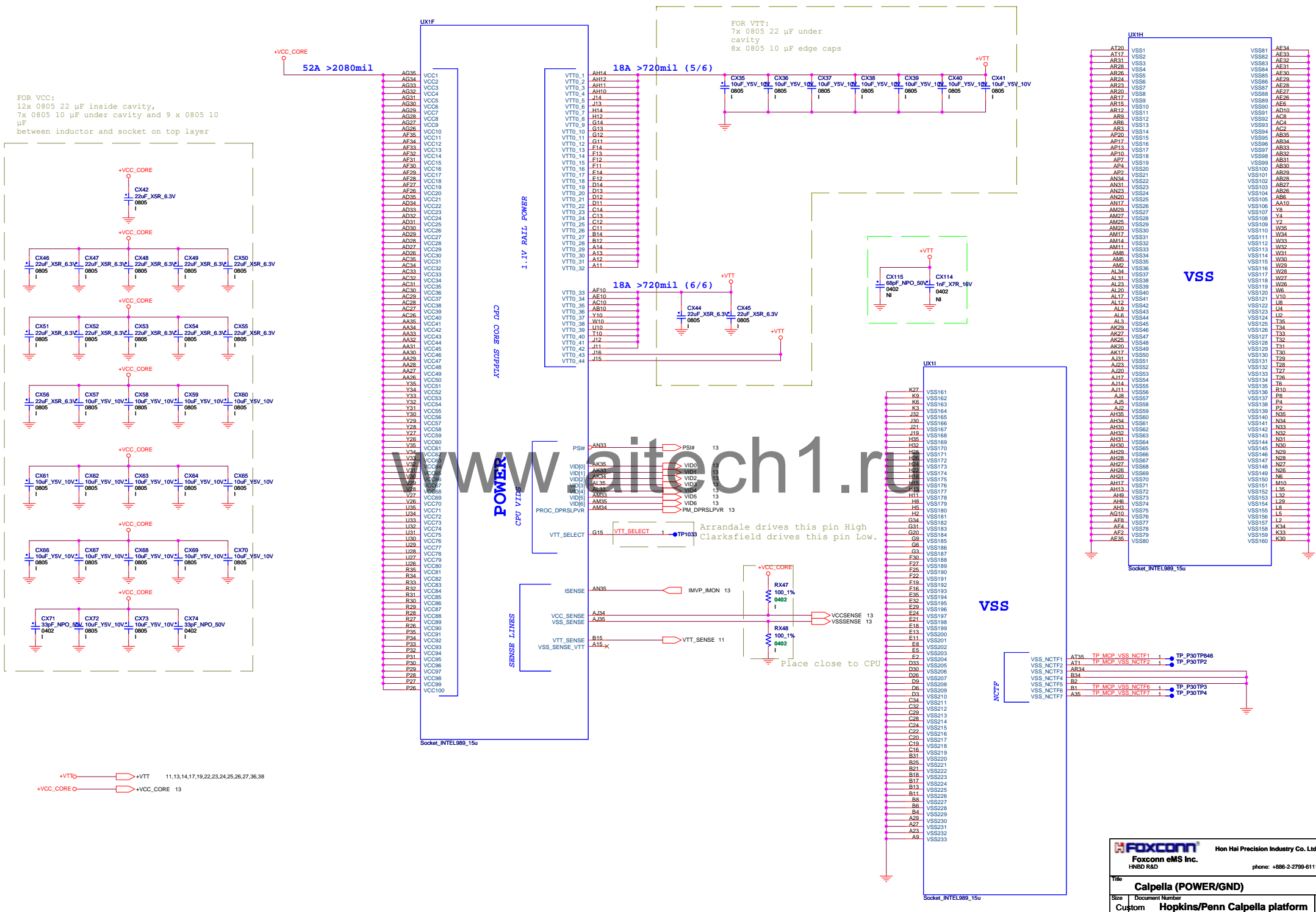
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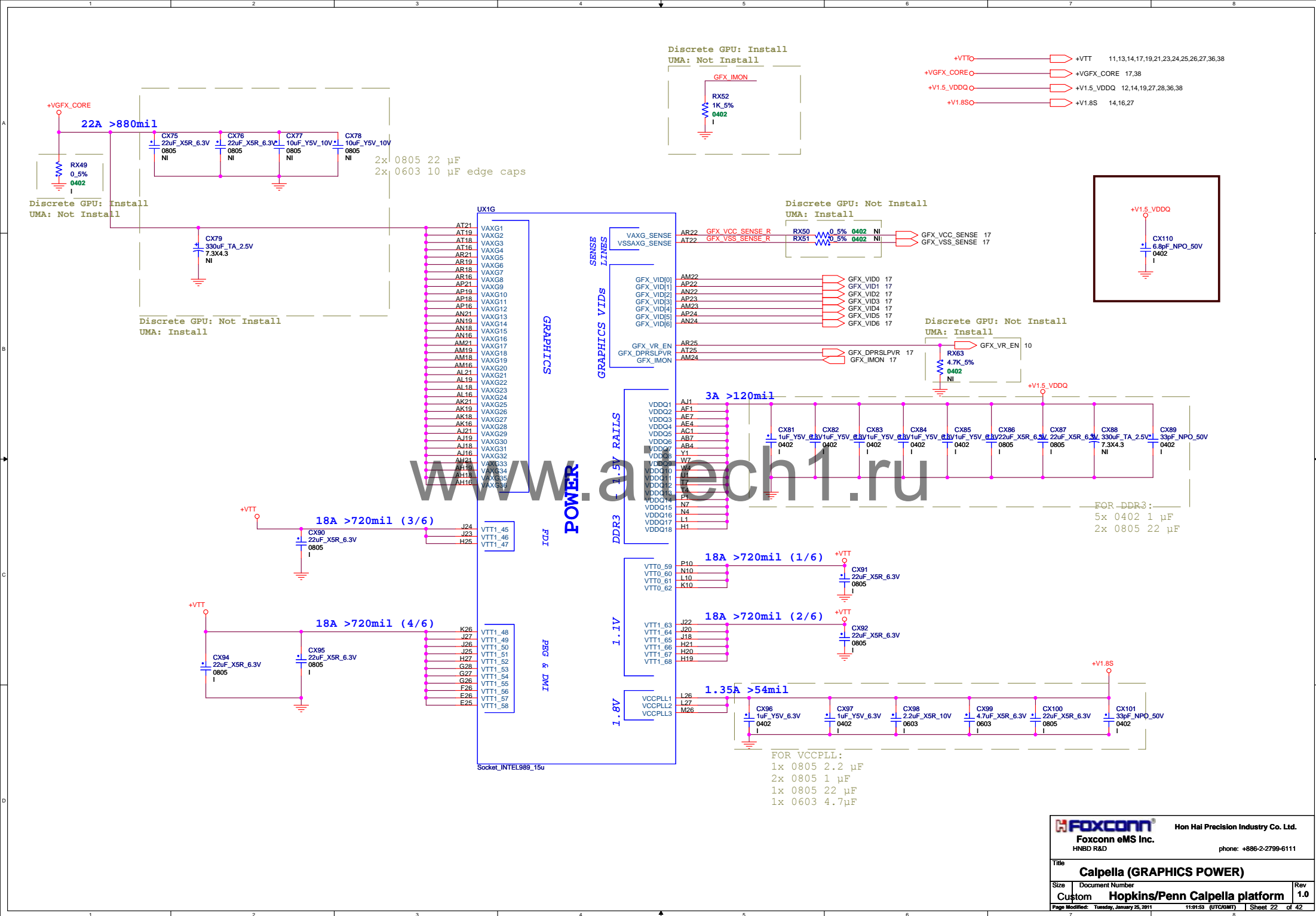
+VGFX POWER SUPPLY

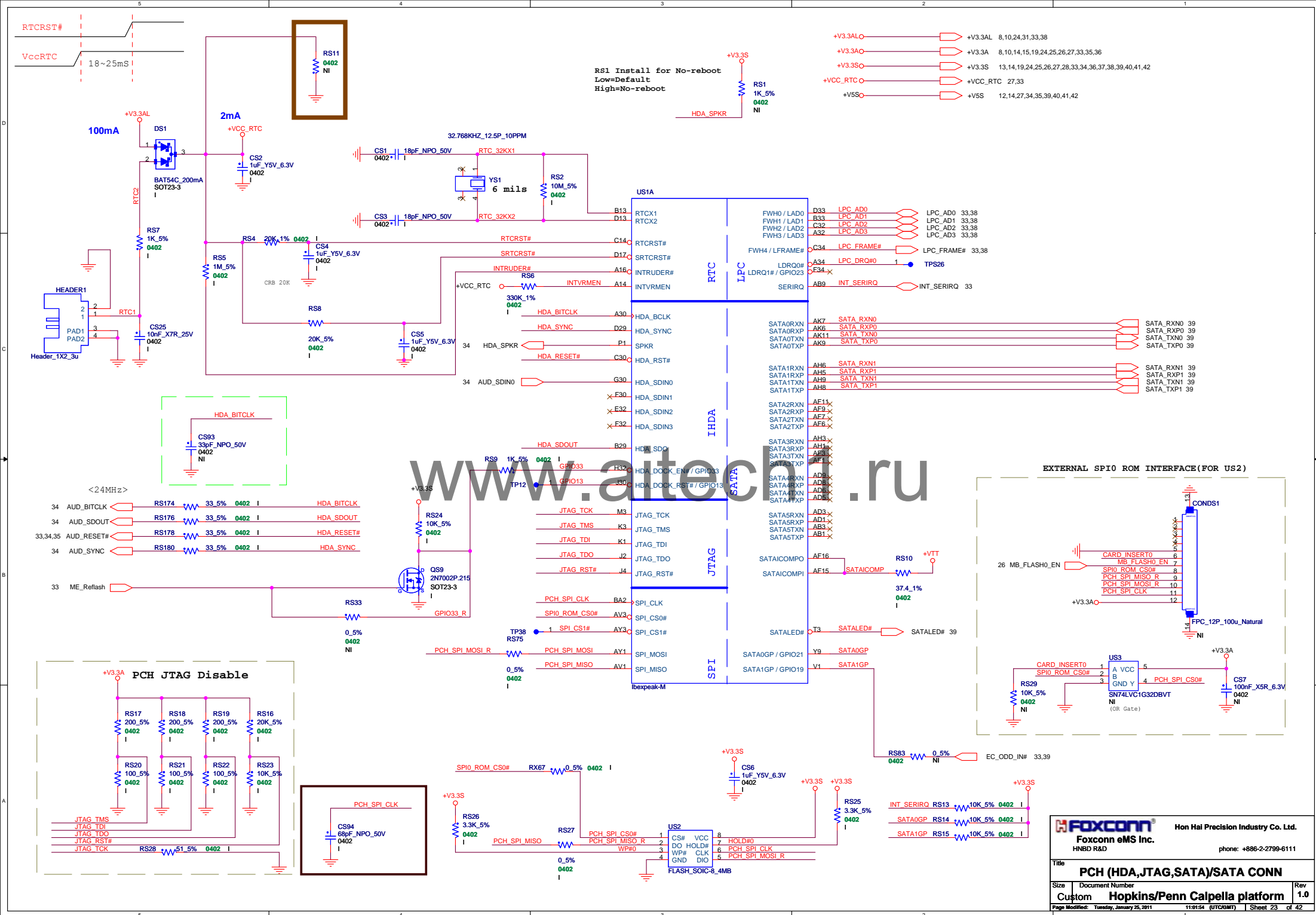
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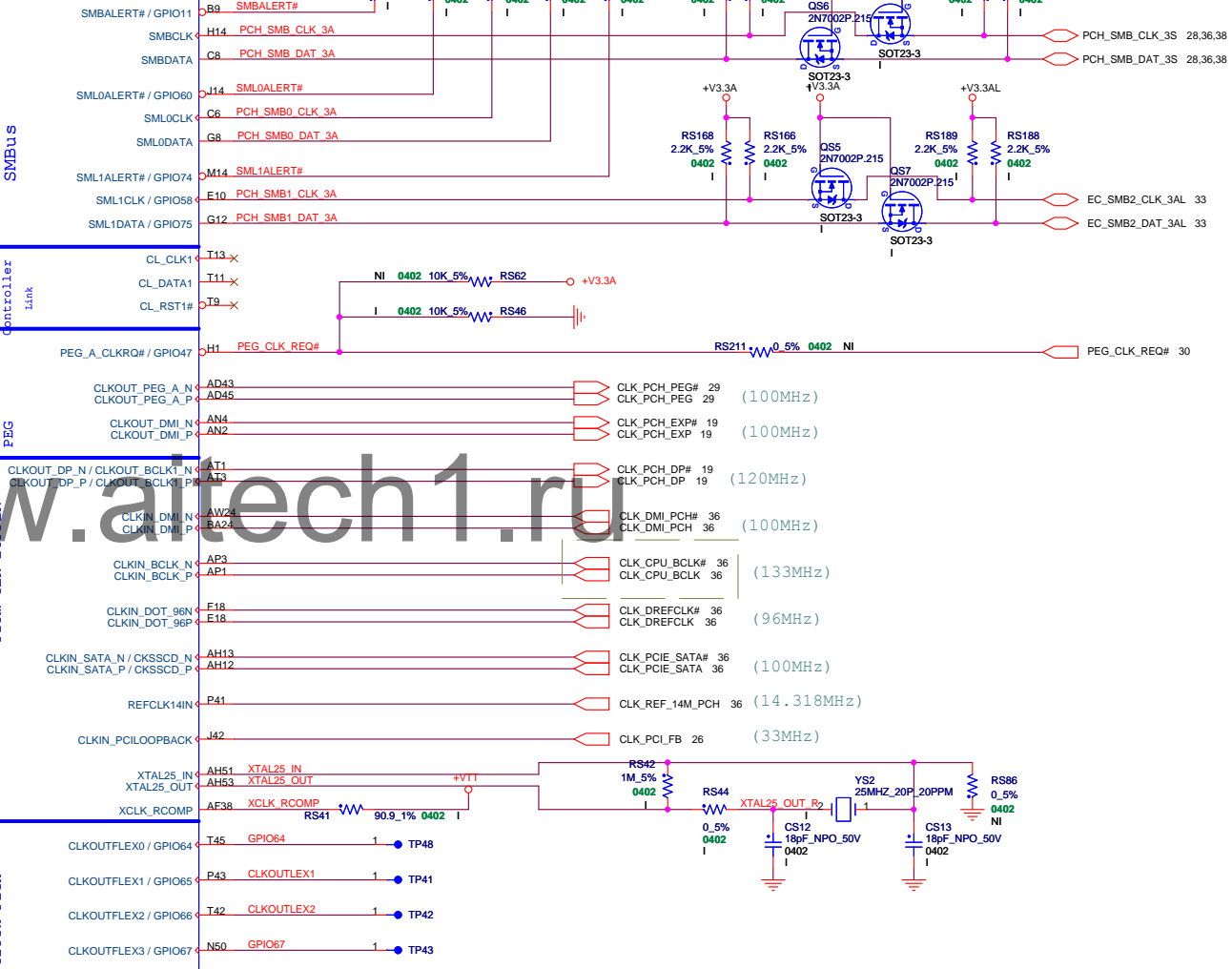
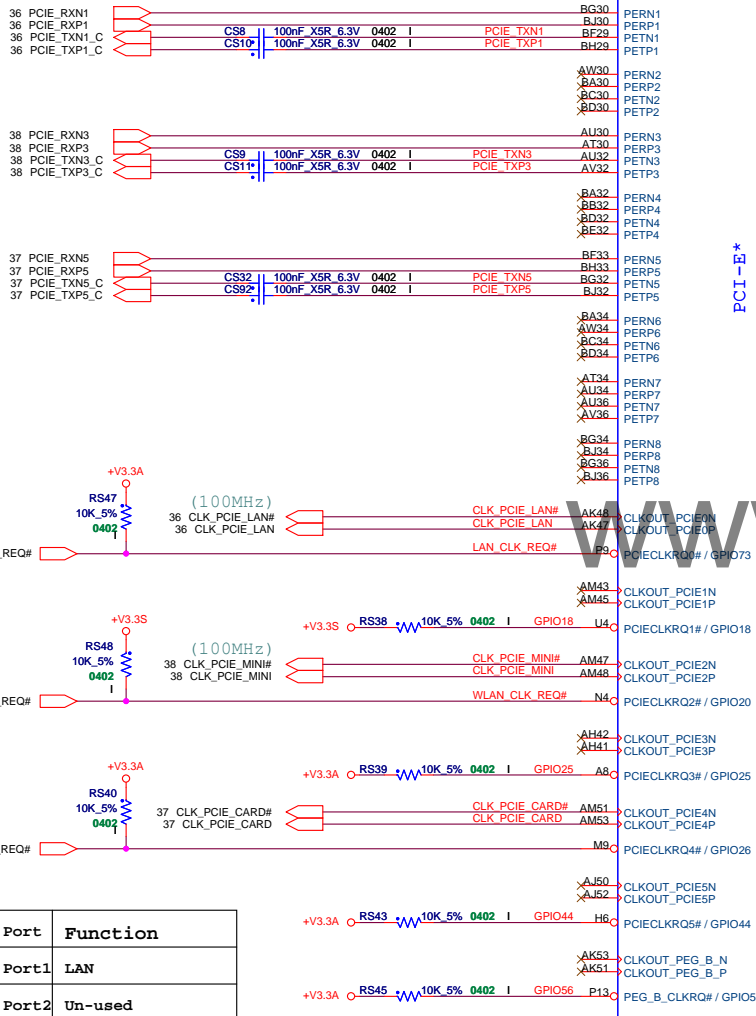






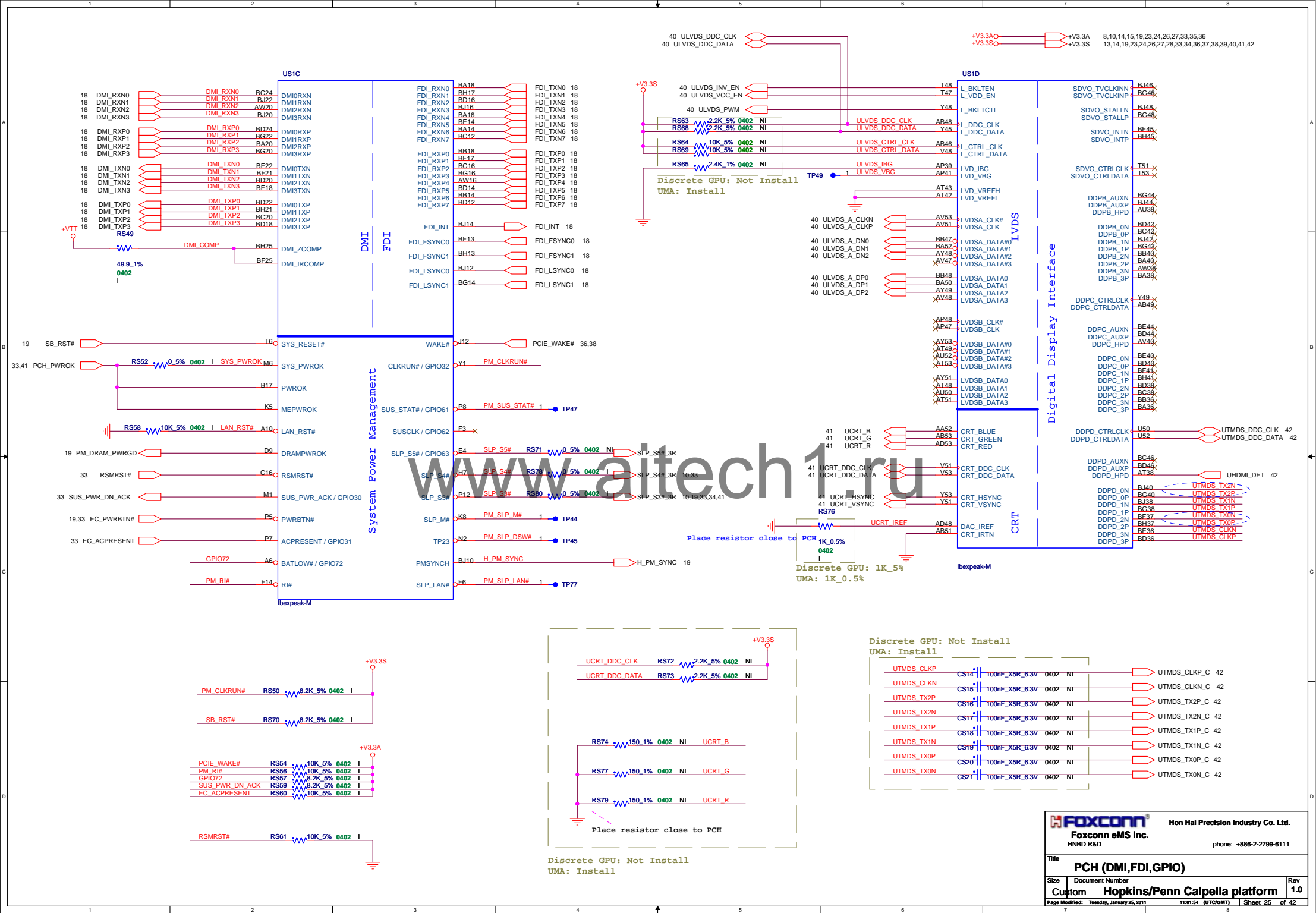


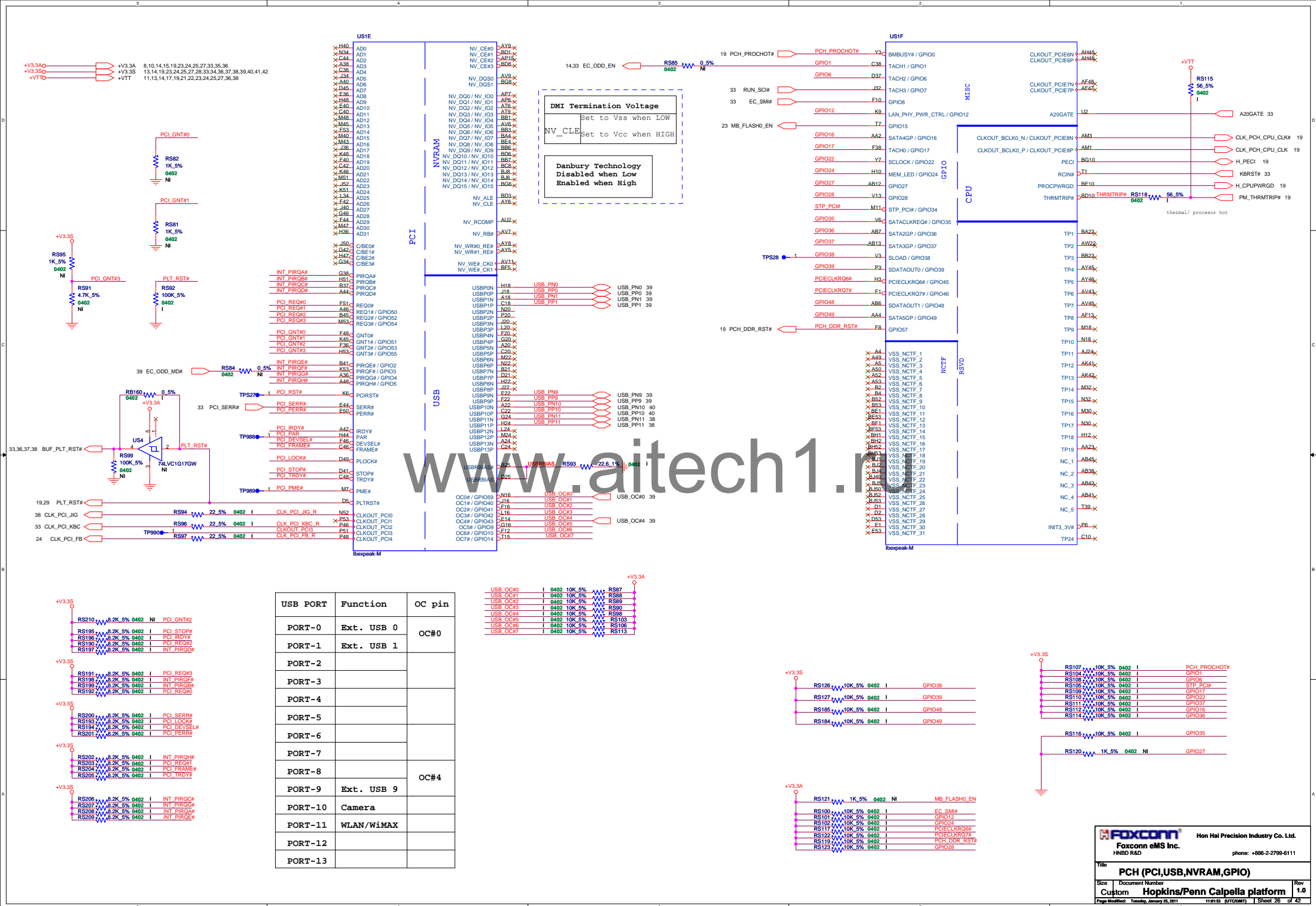


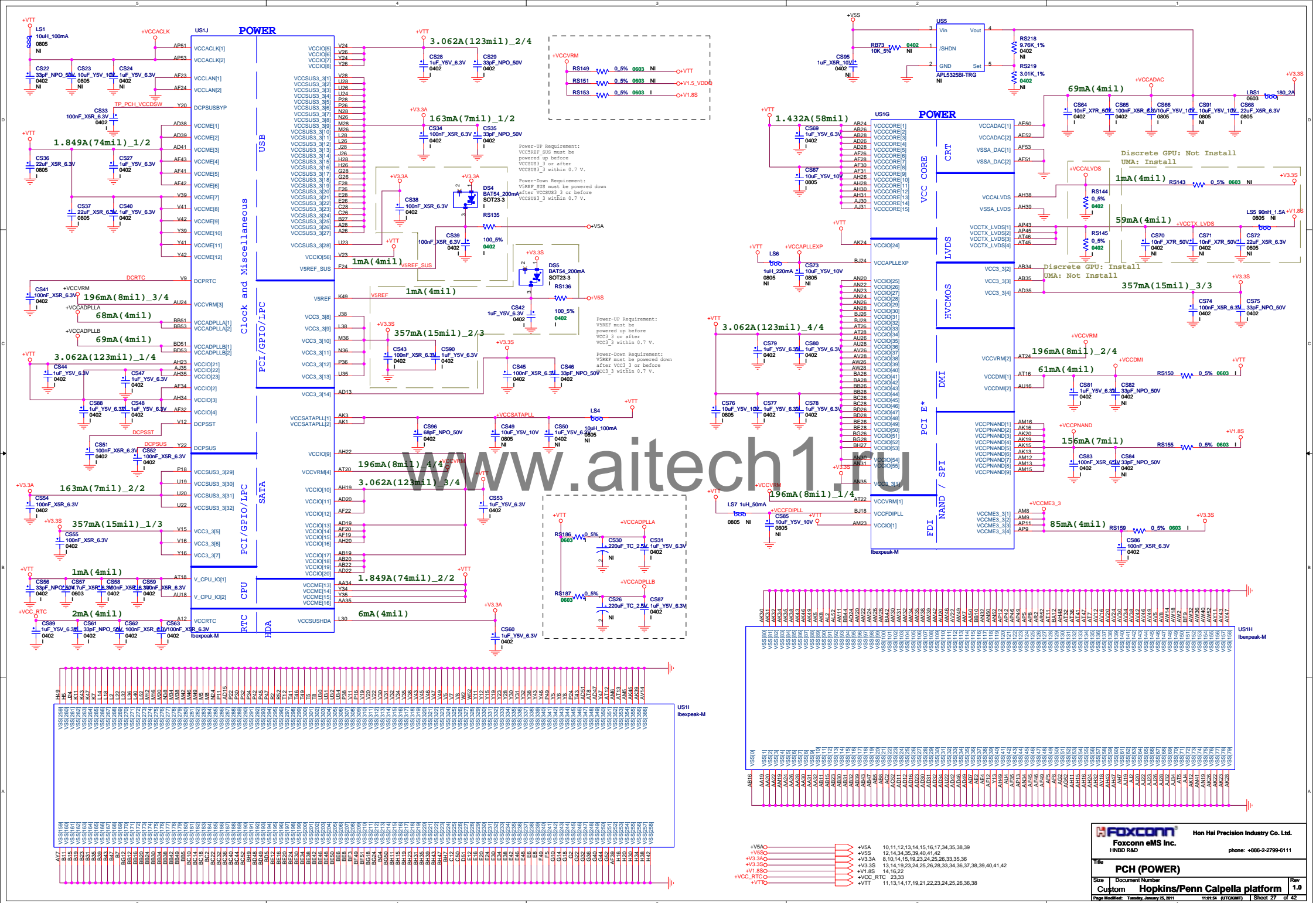


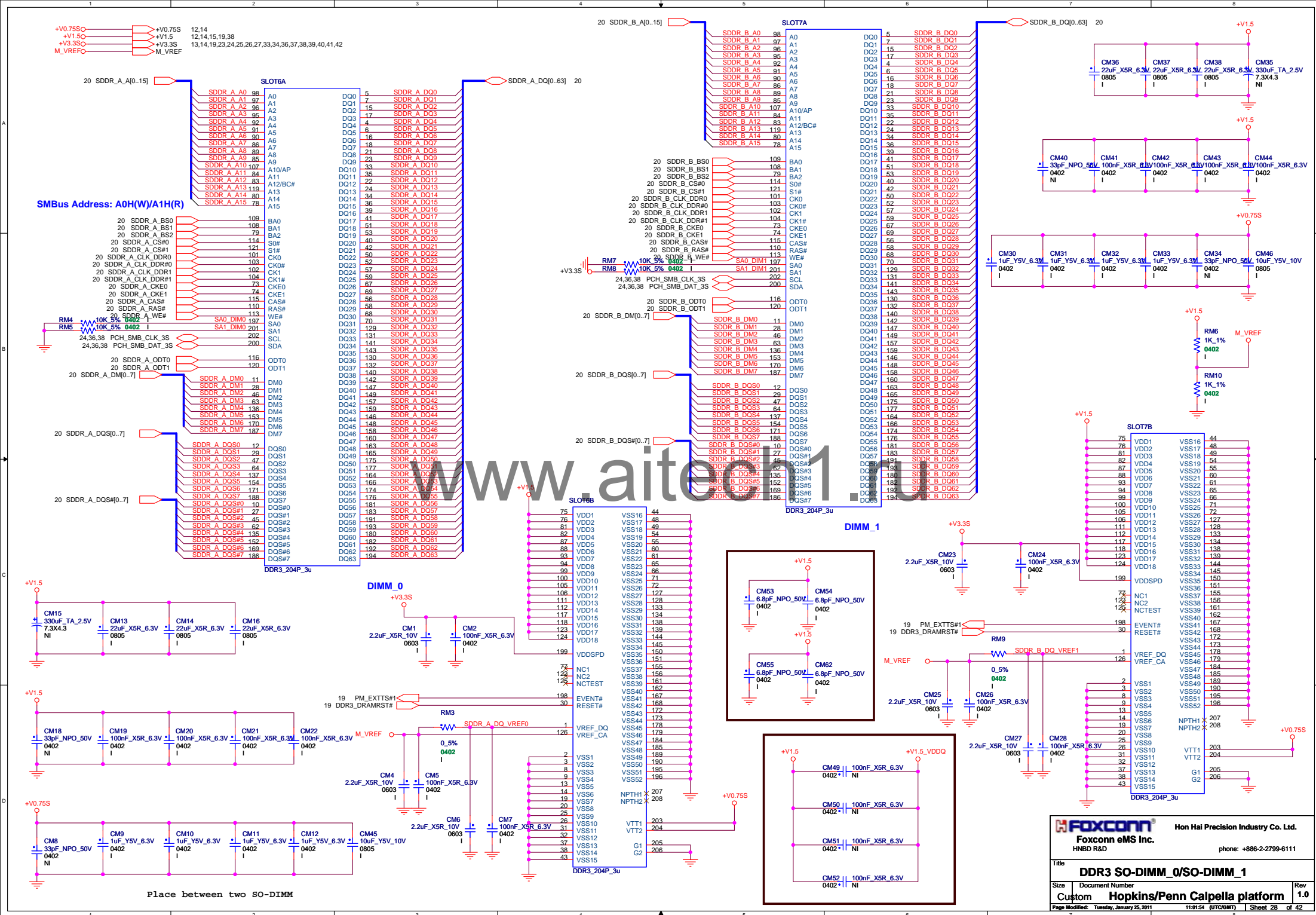
Port	Function
Port1	LAN
Port2	Un-used
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

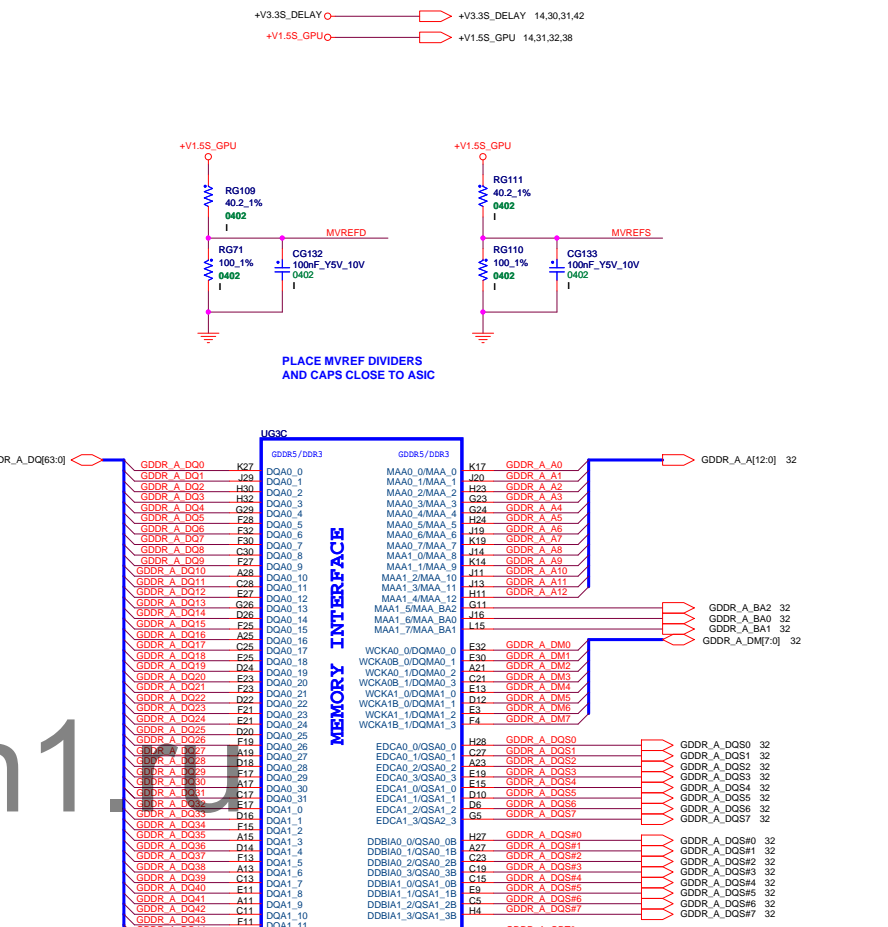
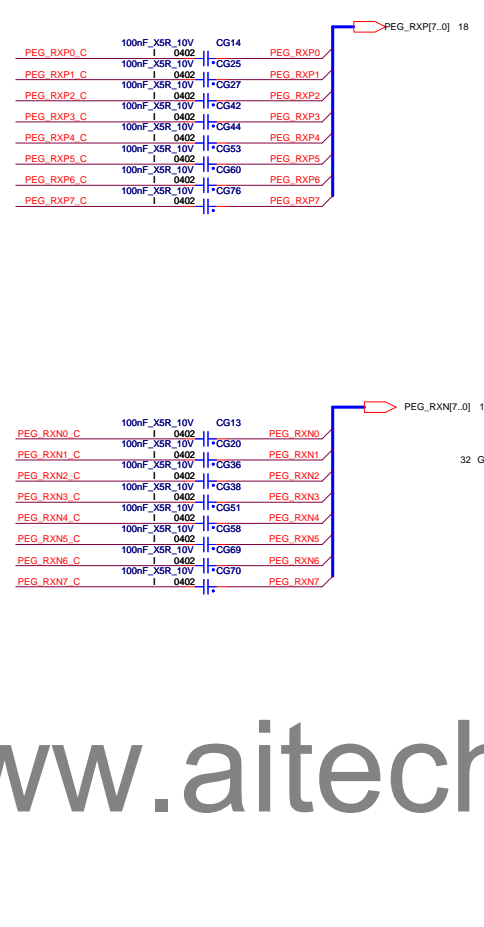
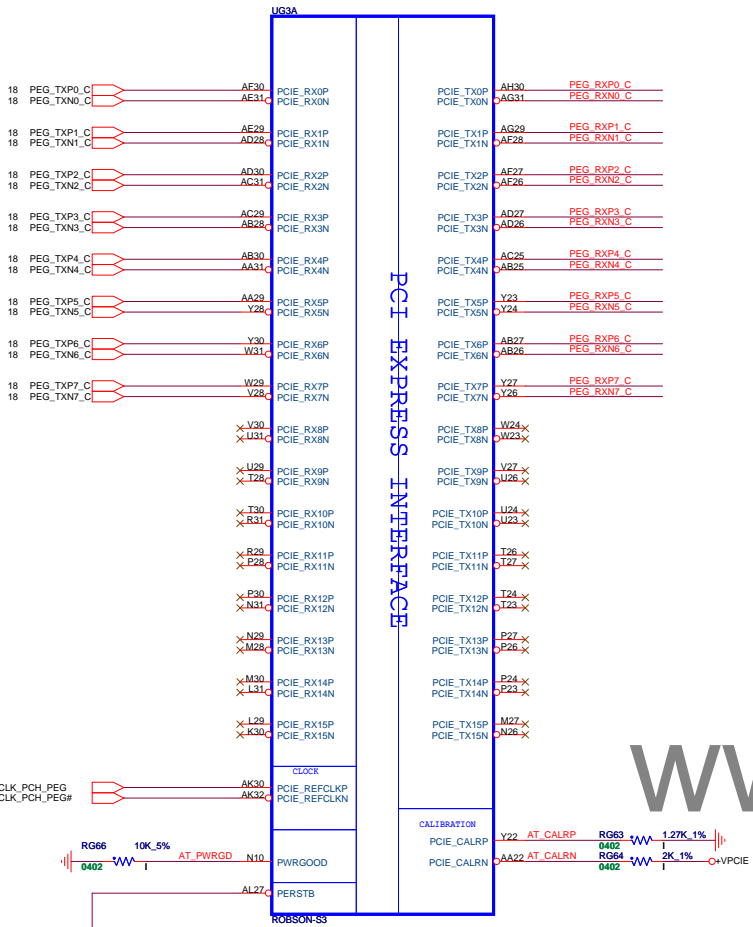
PCI-E Port Table



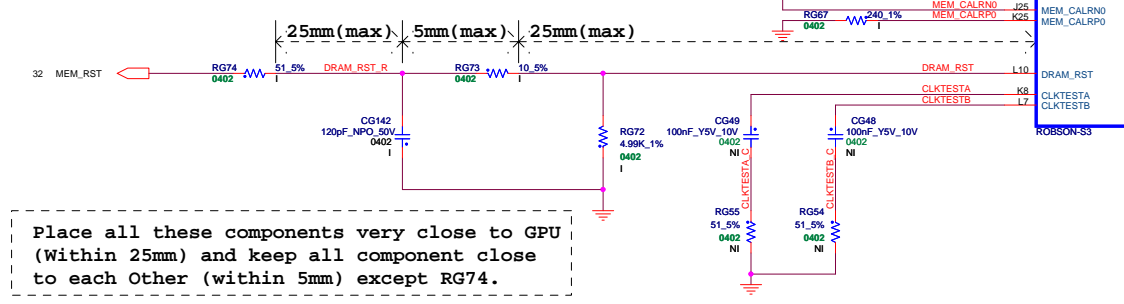


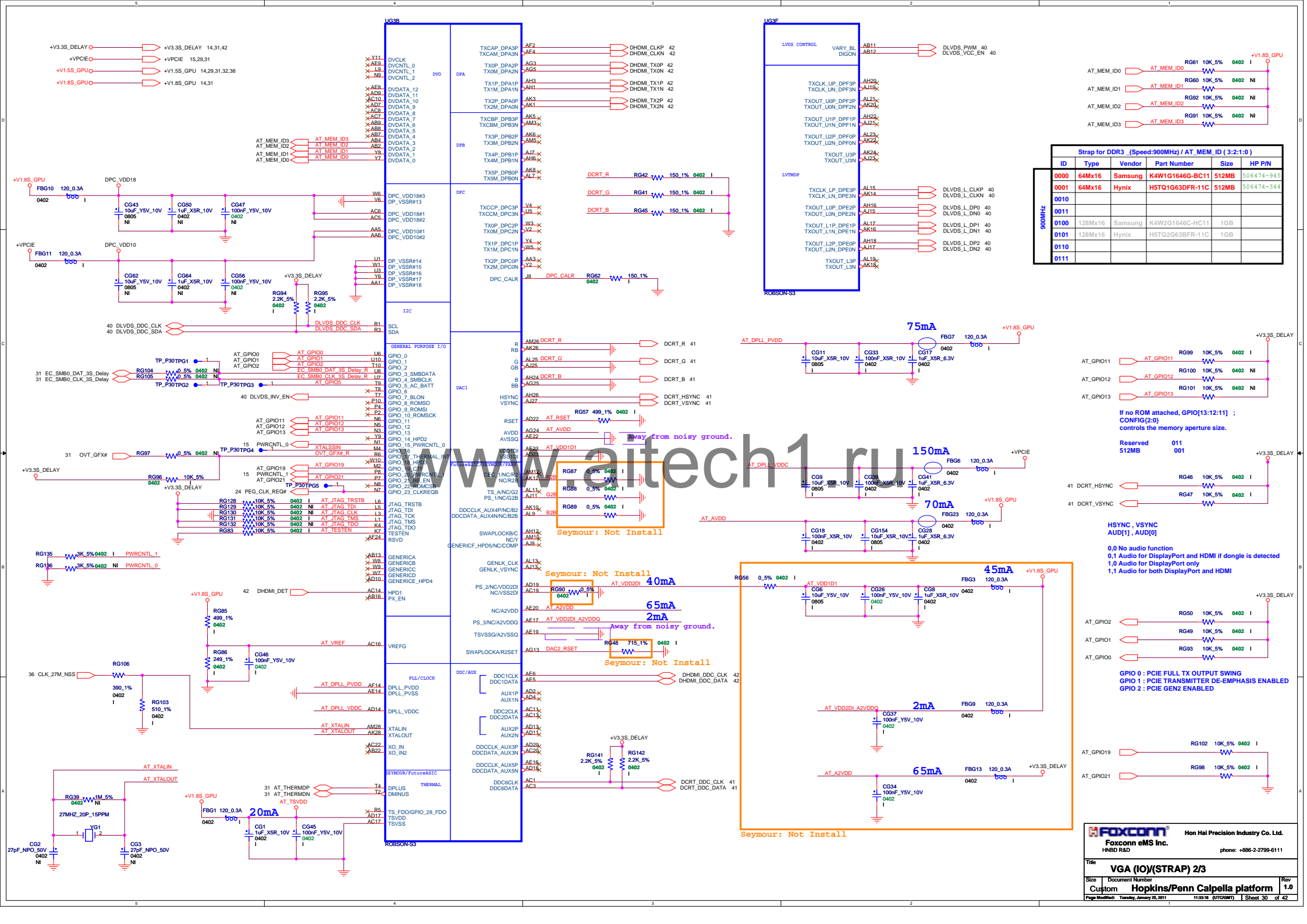






This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.





Strap for DDR3 (Speed:900MHz) / AT_MEM_ID (3:2:1:0)						
ID	Type	Vendor	Part Number	Size	HP	P/N
0000	64Mx16	Samsung	K4W1G1646G-BC11	512MB	506474-943	
0001	64Mx16	Hynix	H5TQ1G63DFR-11C	512MB	506474-344	
0010						
0011						
0100	128Mx16	Samsung	K4W2G1646G-BC11	1GB		
0101	128Mx16	Hynix	H5TQ2G63BFR-11C	1GB		
0110						
0111						

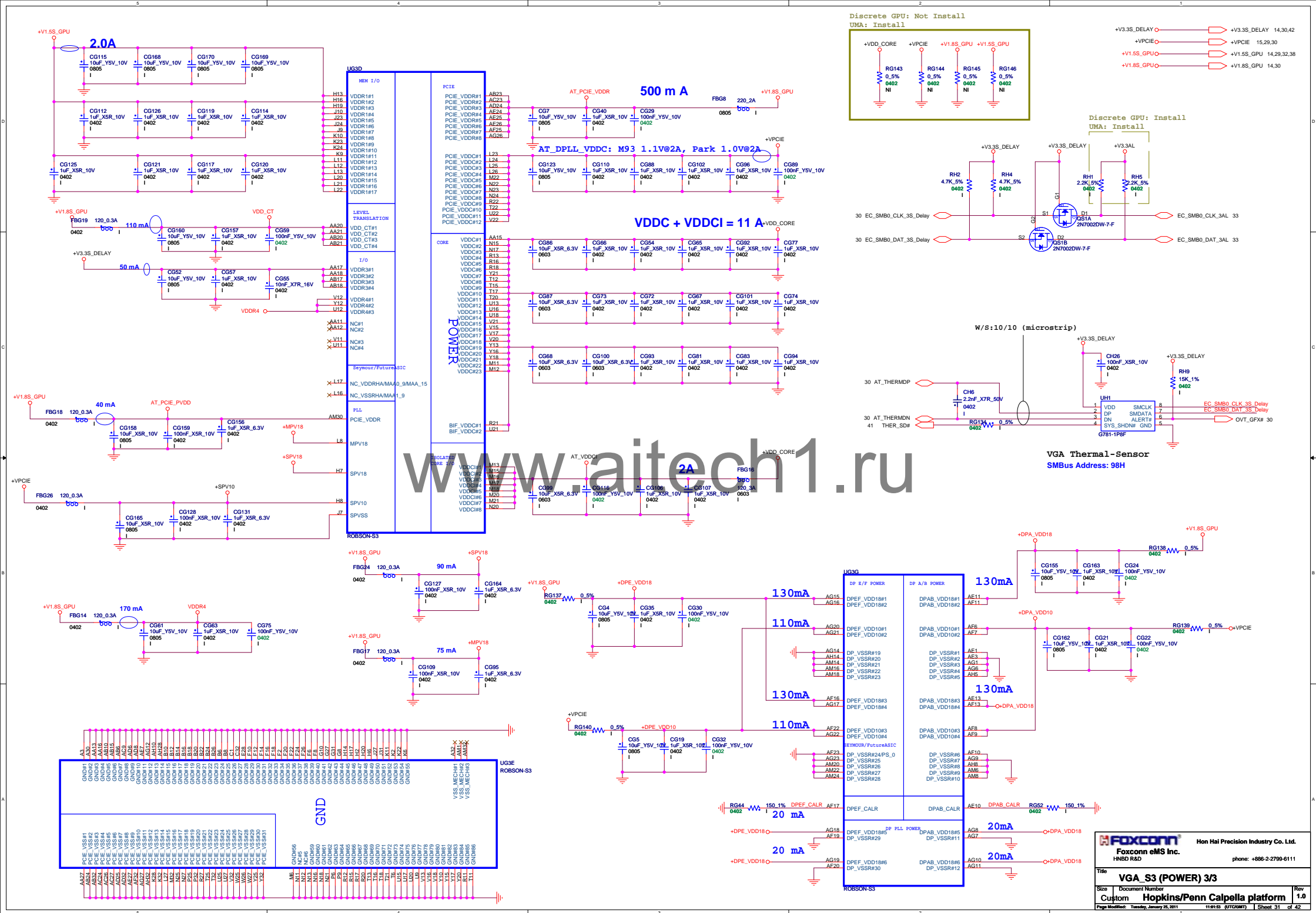
If no ROM attached, GPIO[13:12:11] ; CONFIG(2:0) controls the memory aperture size.

Reserved 011 001

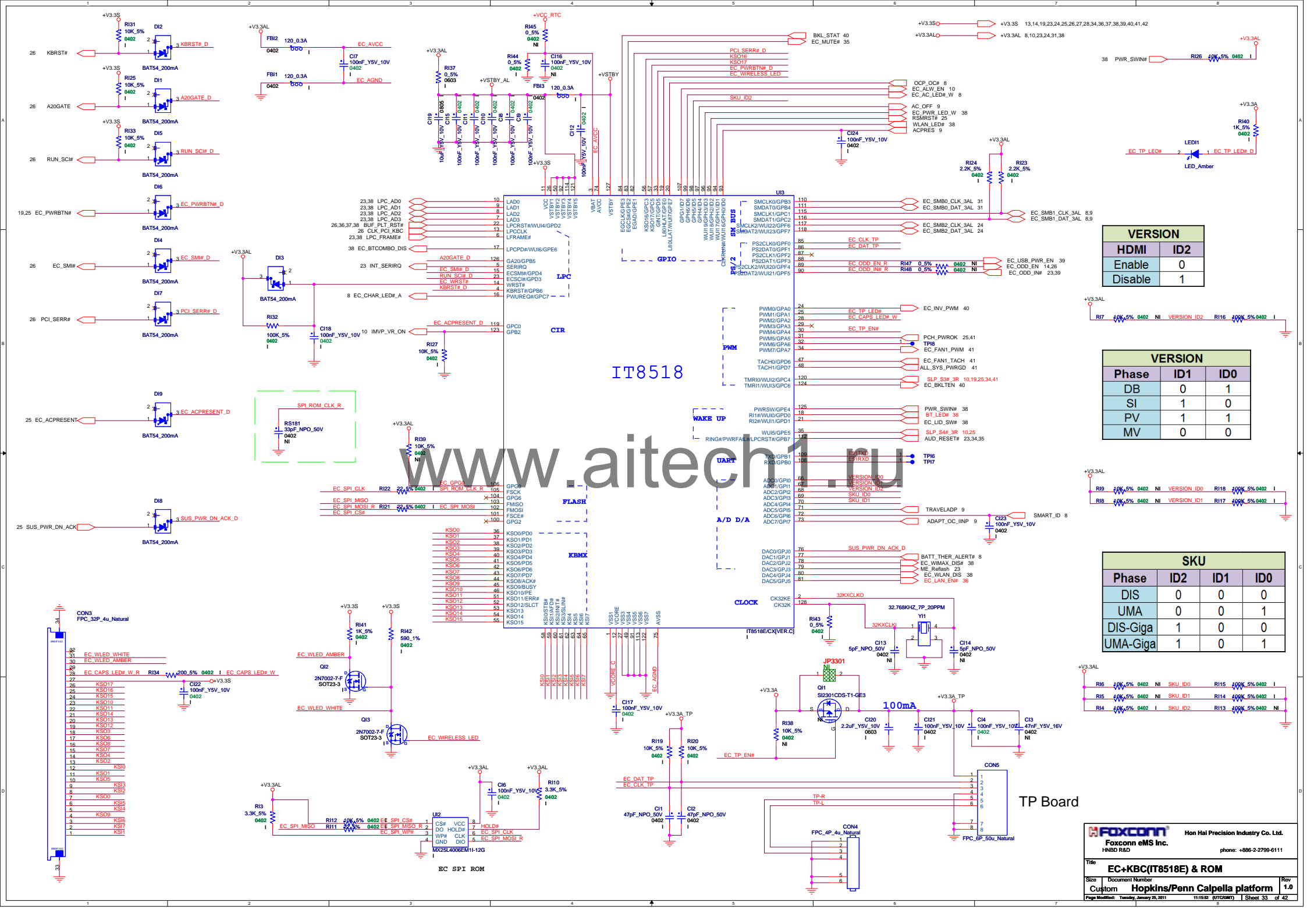
HSYNC , VSYNC
AUD[1] , AUD[0]

0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI

GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED





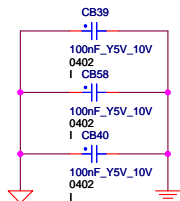
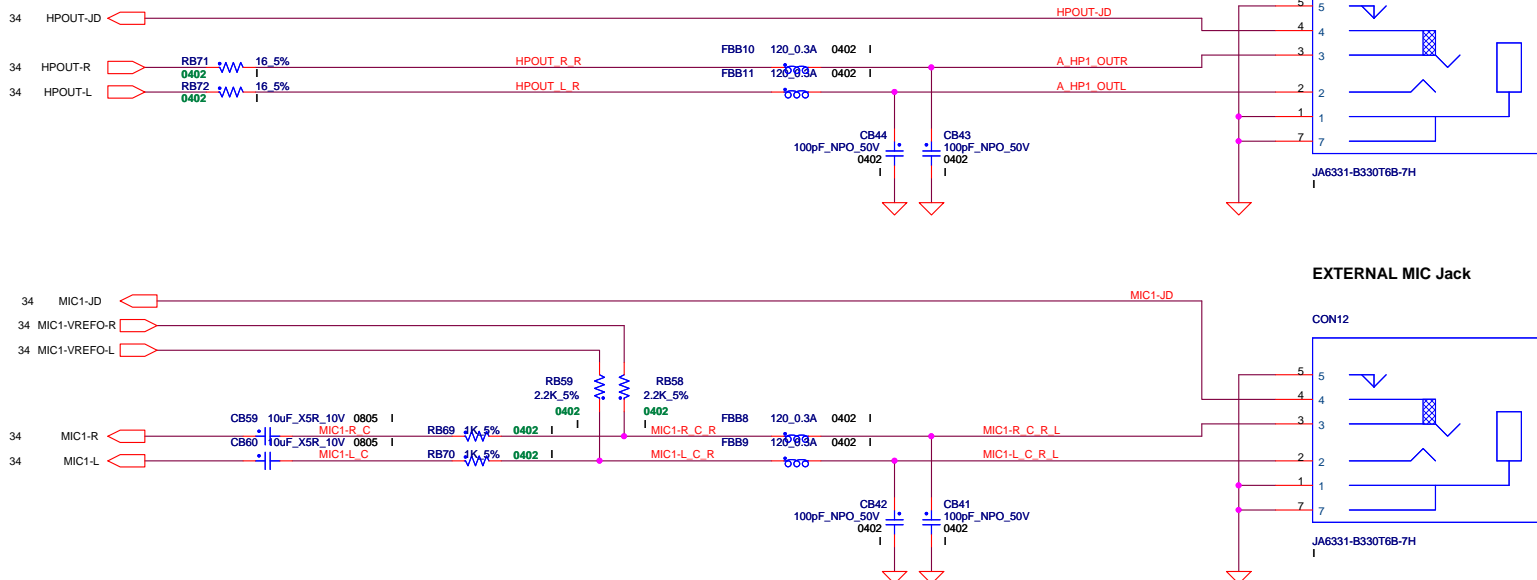


VERSION	
HDMI	ID2
Enable	0
Disable	1

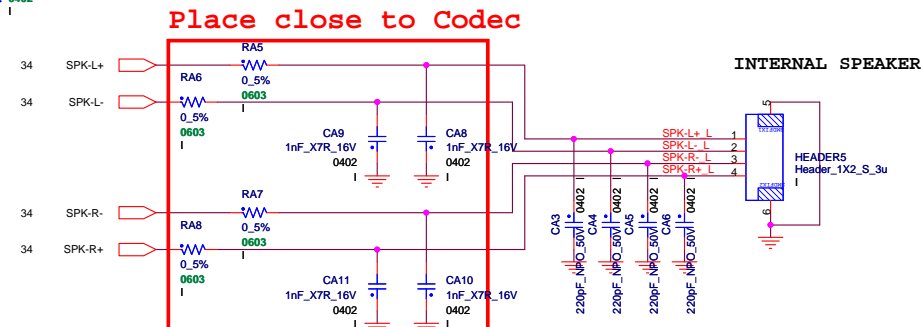
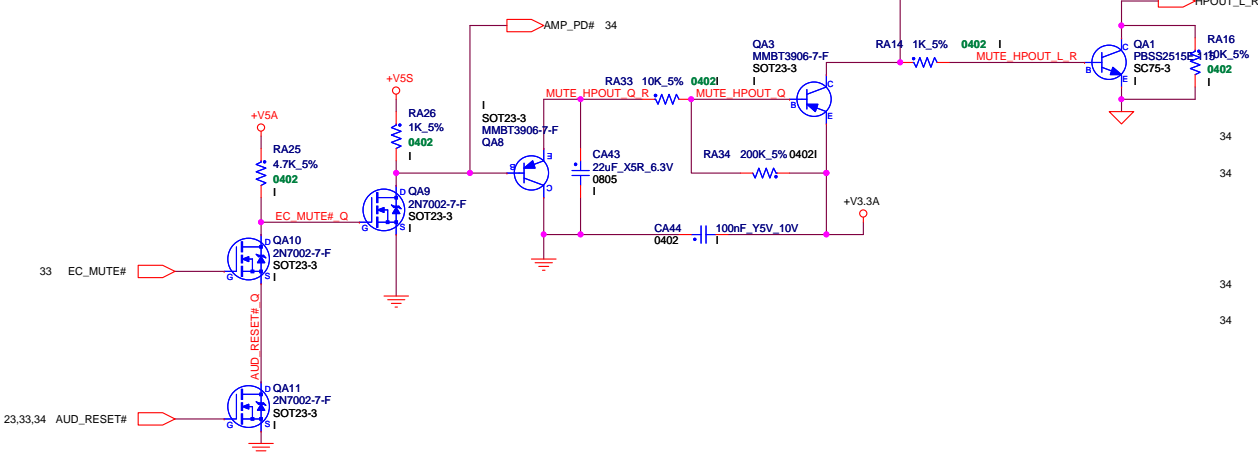
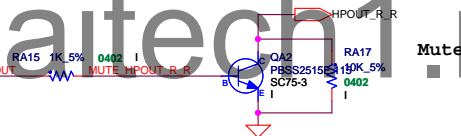
VERSION			
Phase	ID1	ID0	
DB	0	1	
SI	1	0	
PV	1	1	
MV	0	0	

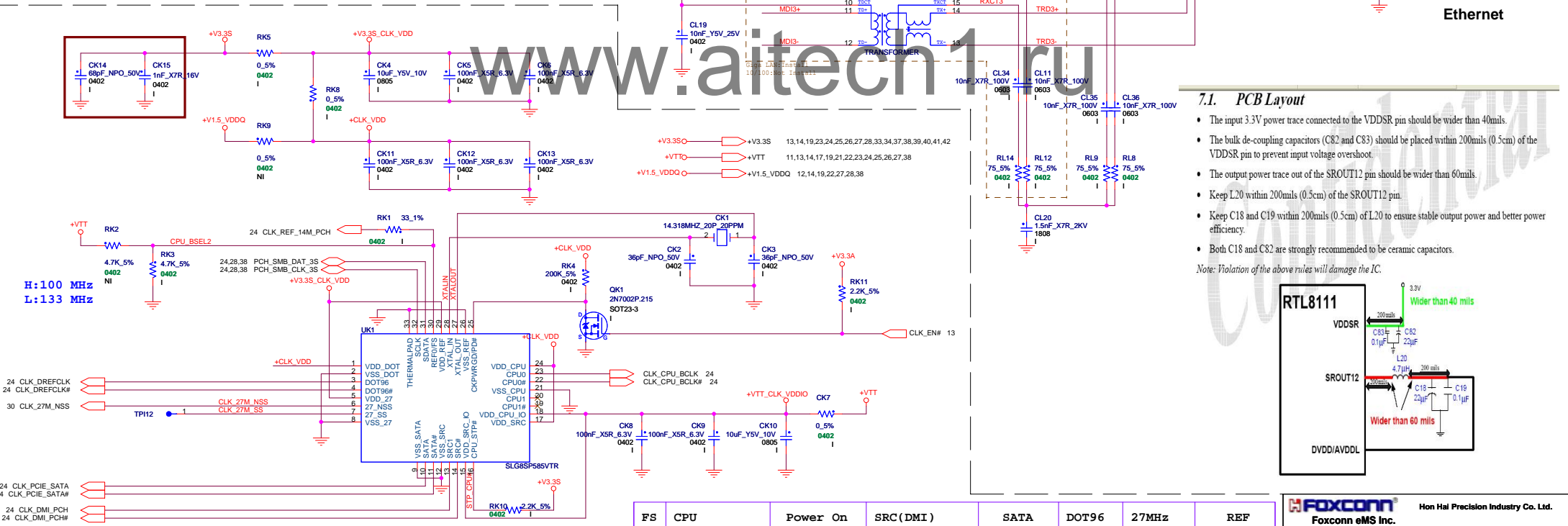
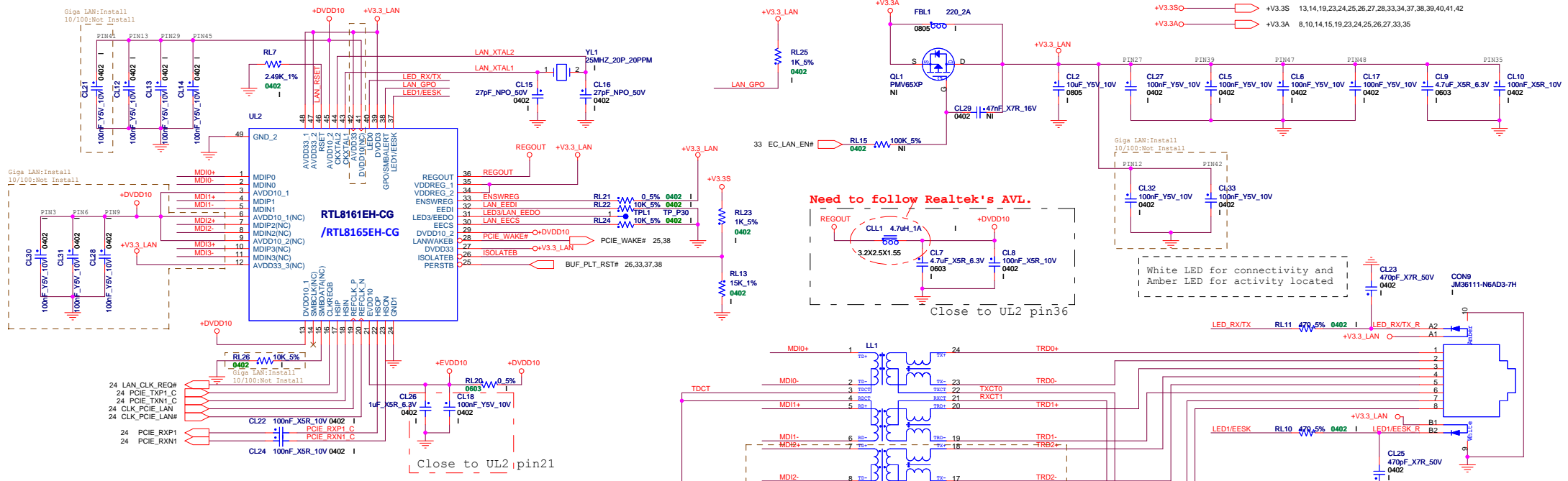
SKU			
Phase	ID2	ID1	ID0
DIS	0	0	0
UMA	0	0	1
DIS-Giga	1	0	0
UMA-Giga	1	0	1

+VSSO → +VSS 12,14,27,34,39,40,41,42
 +V5AO → +V5A 10,11,12,13,14,15,16,17,27,34,38,39



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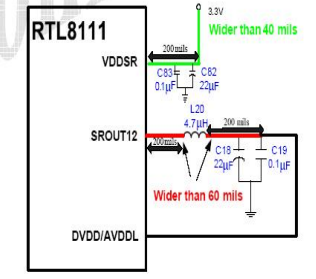


FS	CPU (PCH-->CPU)	Power On	SRC(DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.



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Title

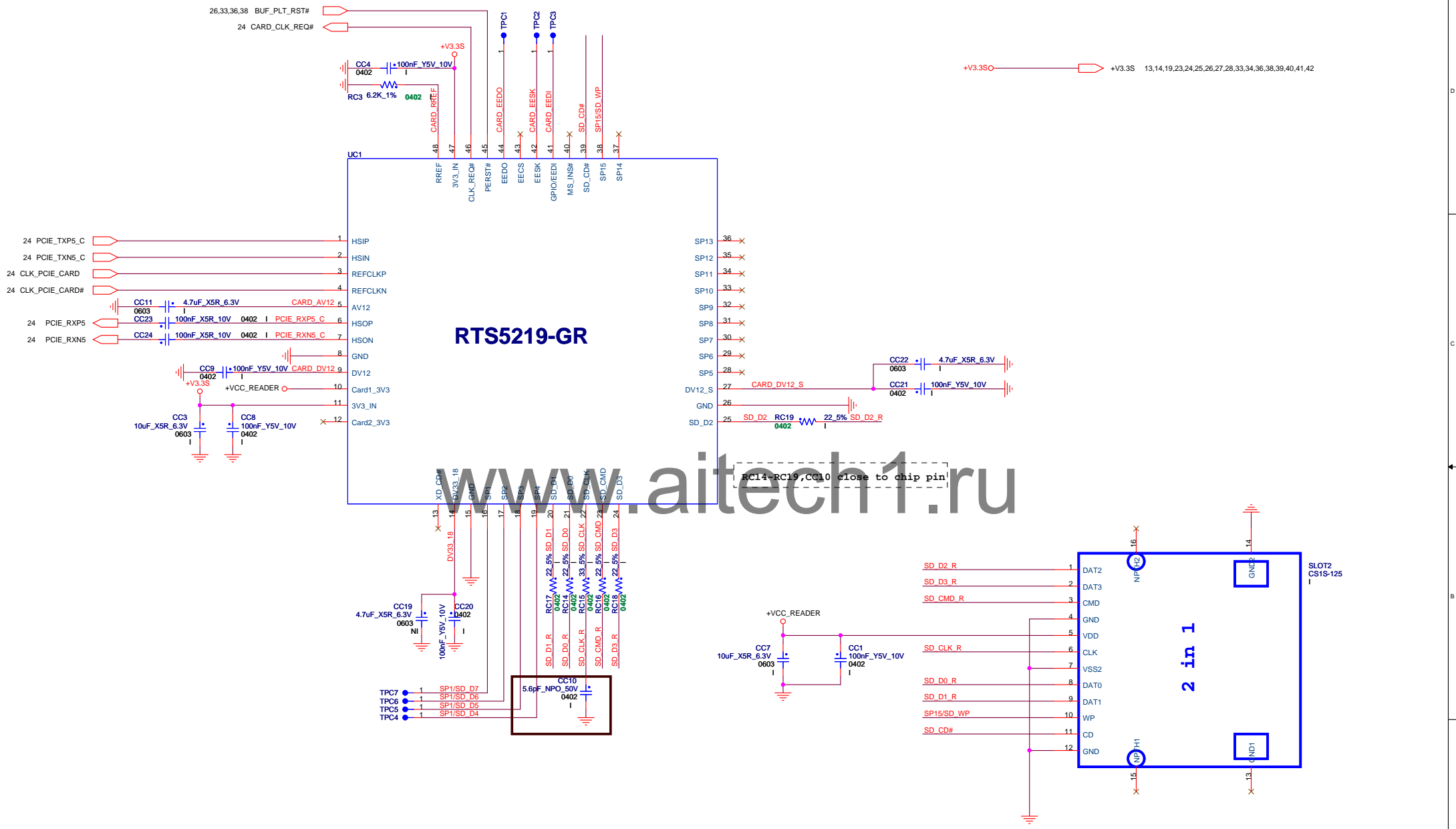
LAN (RTL8161EH)/CLK GEN

Size Document Number

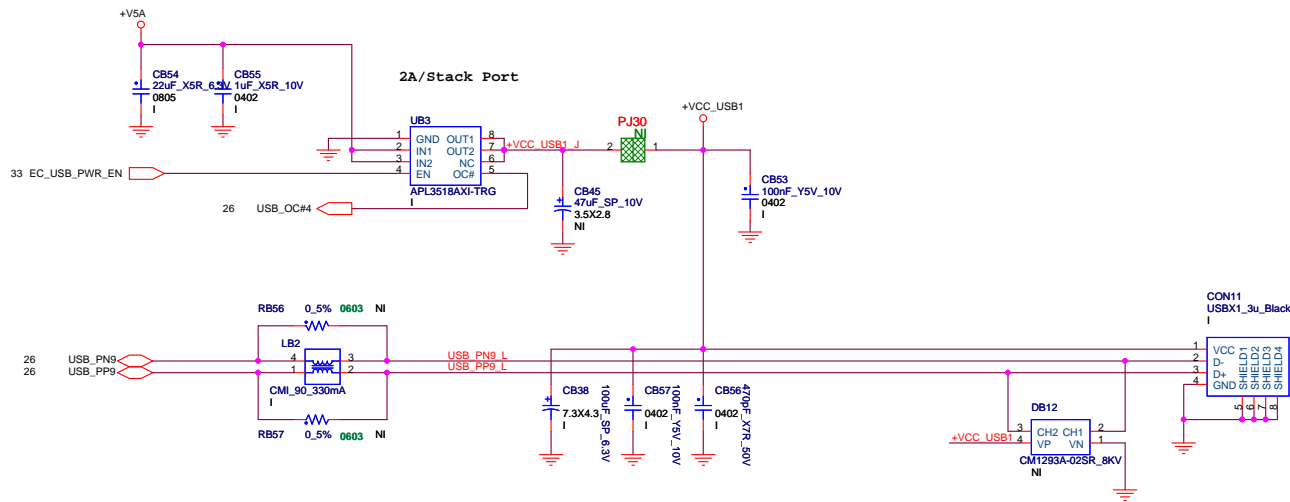
Custom Hopkins/Penn Calpella platform

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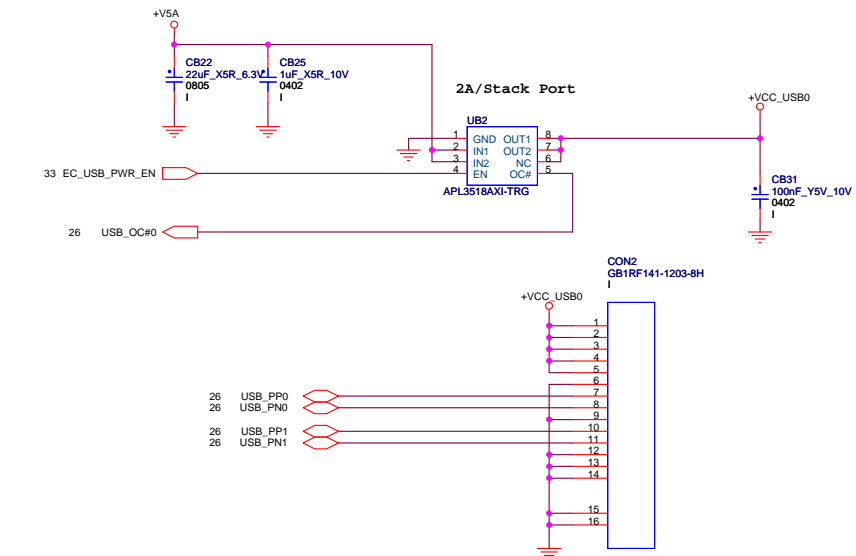
Rev 1.0



USB CONN. X1



USB Board CONN. USB CONN. X2

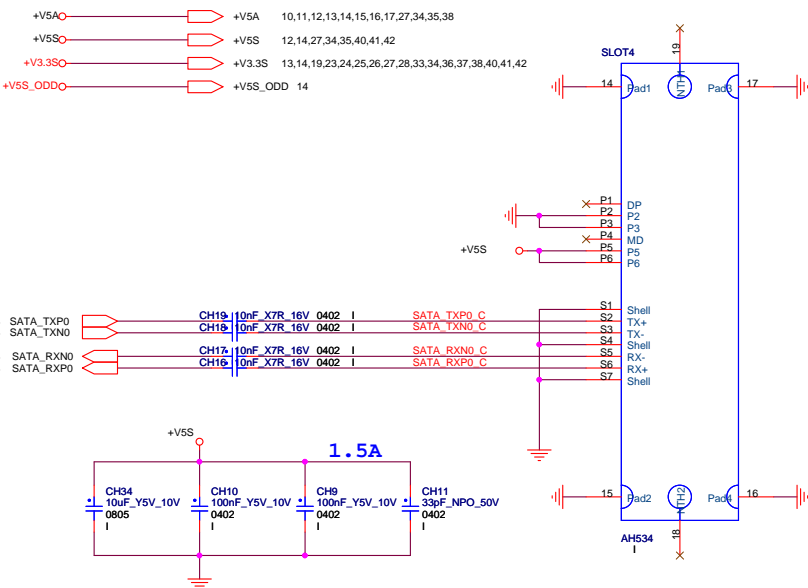


SATA HDD CONN

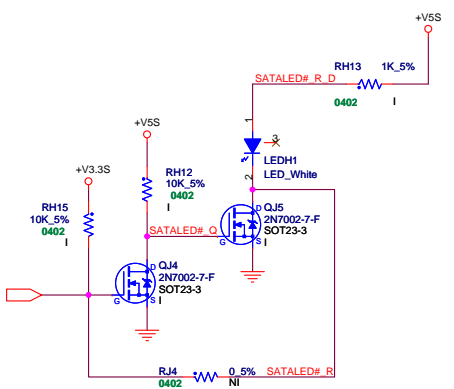
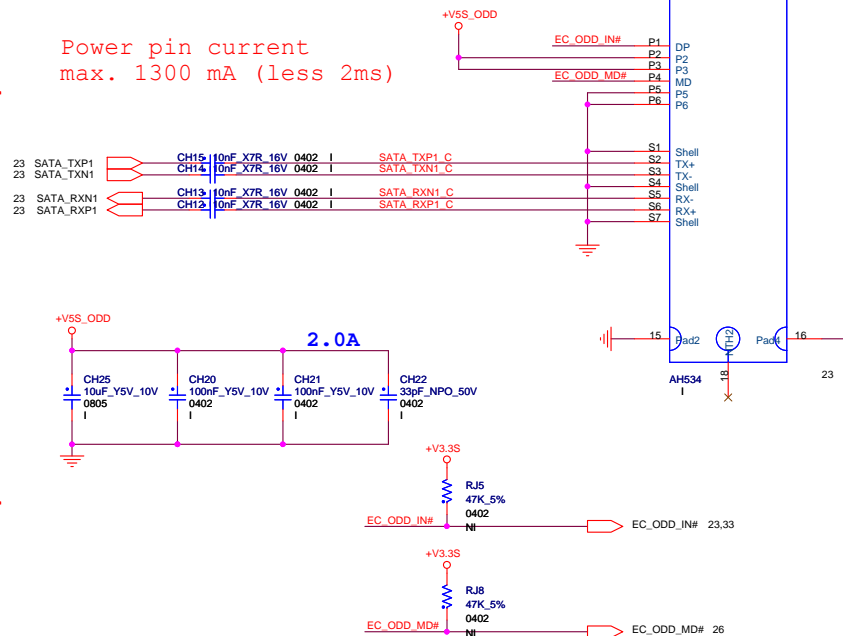
SATA ODD CONN

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HDD/ODD Status LED

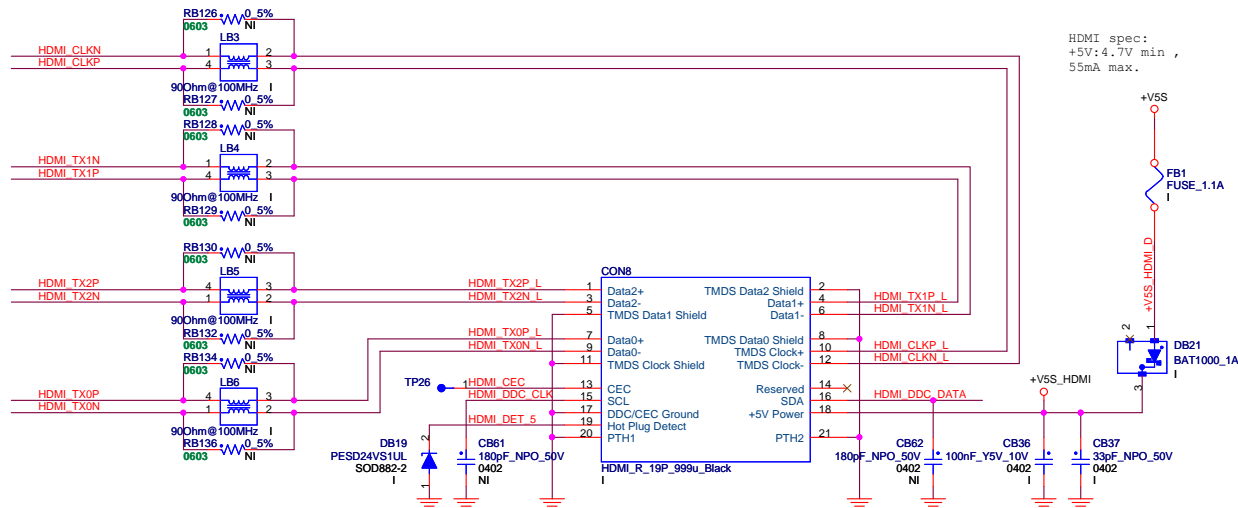
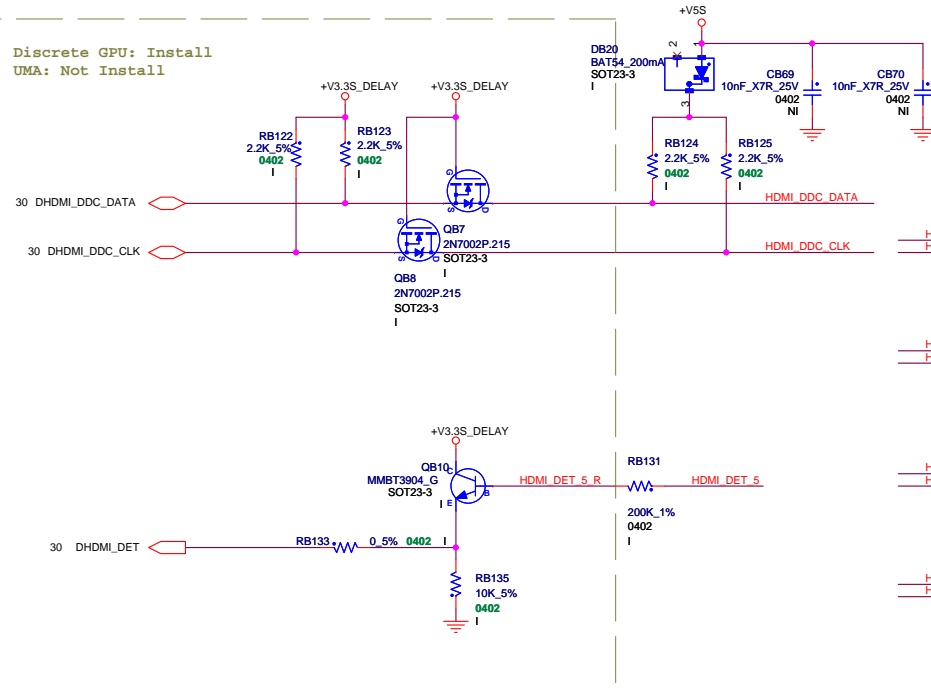


Power pin current
max. 1300 mA (less 2ms)



 Foxconn eMS Inc. HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Title USBX2/USB DB CONN./SATA CONN.			
Size	Document Number	Customer	Rev
Custom		Hopkins/Penn Calpella platform	1.0
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Discrete GPU: Install
UMA: Not Install



Discrete GPU: Not Install
UMA: Install

